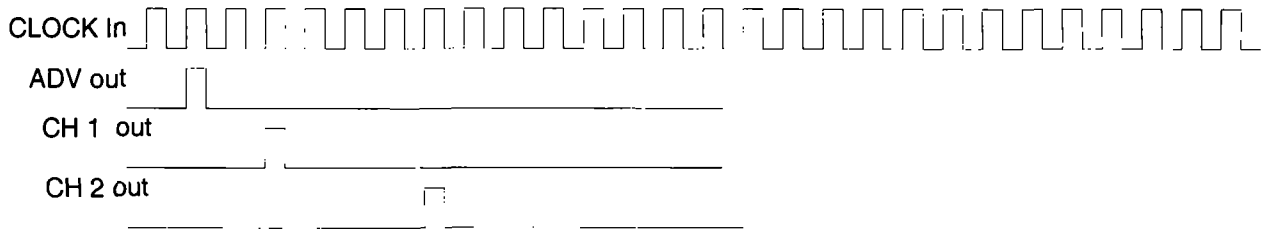
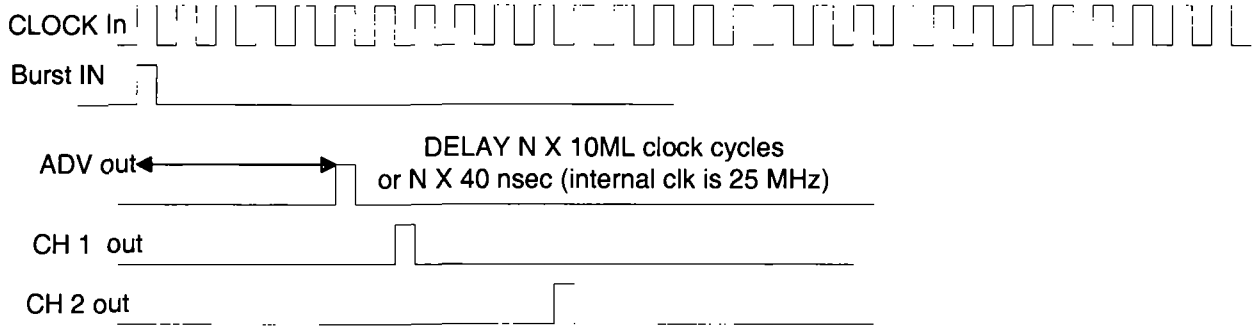


DIVIDE BY      DELAY 1 (NS)    DELAY 2 (NS)

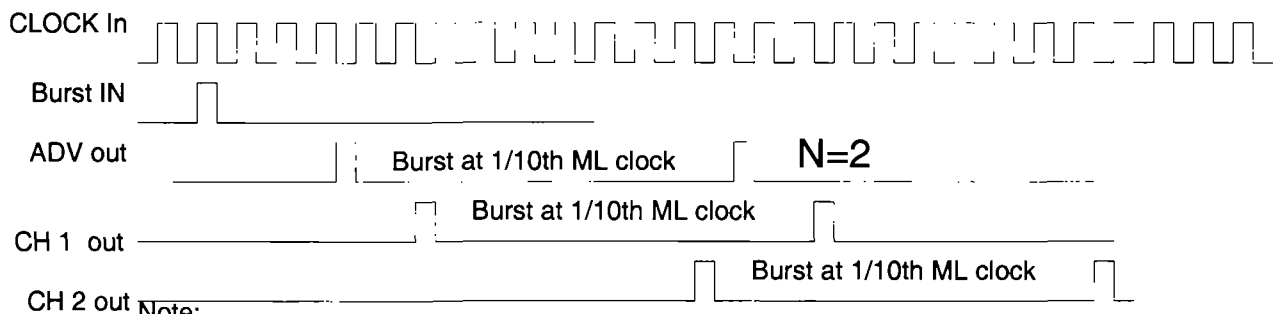
DIVIDE MODE    **999999**    **99**    **999**



**DELAY MODE**



**Burst Mode**



Note:  
 CLOCK In can be external 1-200MHz or or internal clock  
 If EXT ML clock is **not** phase synchronous with ext Burst/Gate IN  
 then Jitter on output is +/- 1/2 ML clock cycle

**DD1 Unit Typical Timing**