DIVIDE BY 999999 99 999

CLOCK In
ADV out
CH 1 out
CH 2 out

DELAY MODE

CLOCK In
Burst IN
ADV out
DELAY N X 10ML clock cycles or N X 40 nsec (internal clk is 25 MHz)
CH 1 out
CH 2 out

Burst Mode

CLOCK In
Burst IN
ADV out
Burst at 1/10th ML clock
N=2
Burst at 1/10th ML clock
Burst at 1/10th ML clock

DD1 Unit Typical Timing

Note:
CLOCK In can be external 1-200MHz or or internal clock
If EXT ML clock is not phase synchronous with ext Burst/Gate IN
then Jitter on output is +/- 1/2 ML clock cycle