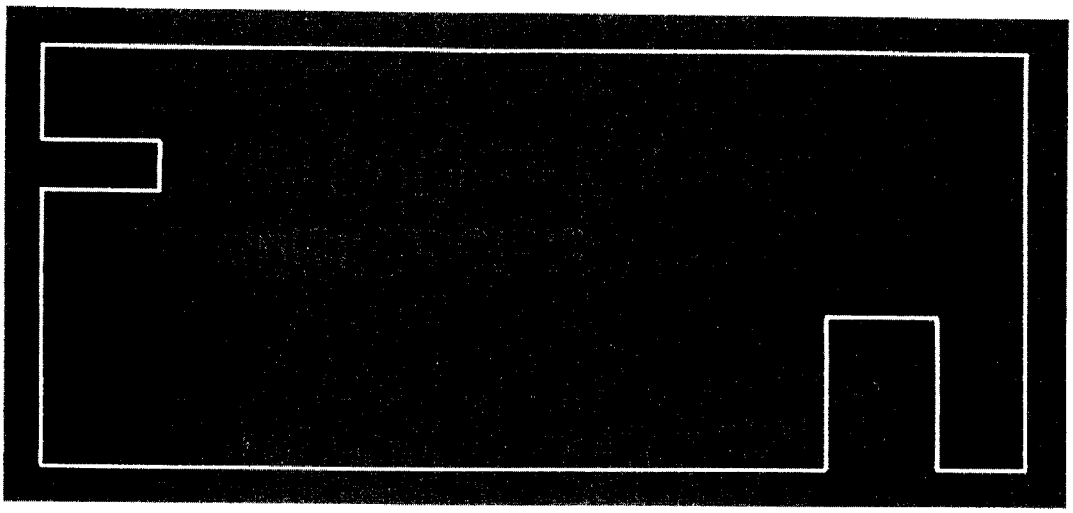


INTRODUCTION

Field-effect transistors (FETs) are different from the ordinary transistors (sometimes called "bipolar transistors," "bipolar junction transistors," or BJTs, to distinguish them from FETs) that we talked about in the last chapter. Broadly speaking, however, they are similar devices, which we might call *charge-control devices*: In both cases we have a 3-terminal device in which the conduction between two electrodes depends on the availability of charge carriers, which is controlled by a voltage applied to a third *control electrode.*

Here's how they differ: In an *npn* BJT the collector-base junction is back-biased, so no current normally flows. Forward-biasing the base-emitter junction by $\approx$0.6 volts overcomes its diode "contact potential barrier," causing electrons to enter the base region, where they are strongly attracted to the collector; although some base current results, most of these "minority carriers" are captured by the collector. This results in a collector current, controlled by a (smaller) base current. The collector current is proportional to the rate of injection of minority carriers into the base region, which is an exponential function of the *BE* potential difference (the Ebers–Moll equation). You can think of a bipolar transistor as a current amplifier (with roughly constant current gain, h_{FE}) or as a transconductance device (Ebers–Moll).

In a FET, as the name suggests, conduction in a *channel* is controlled by an *electric field*, produced by a voltage applied to the *gate* electrode. There are no forward-biased junctions, so the gate draws no current; this is perhaps the most important advantage of the FET. As with BJTs, there are two polarities, *n-channel* FETs (conduction by electrons) and *p-channel* FETs (conduction by holes). These two polarities are analogous to the familiar *npn* and *pnp* bipolar transistors, respectively. In addition, however, FETs tend to be confusing at first because they can be made with two different kinds of gates (thus JFETs and MOSFETs), and with two different kinds of channel doping (leading to *enhancement* and *depletion* modes). We'll sort out these possibilities shortly.

First, though, some motivation and perspective: The FET's nonexistent gate current is its most important characteristic. The resulting high input impedance (which can be greater than $10^{14}\Omega$) is essential in many applications, and in any case it makes circuit design simple and fun. For applications like analog switches and amplifiers of ultrahigh input impedance, FETs have no equal. They can be easily used by themselves or combined with bipolar transistors to make integrated circuits: In the next chapter we'll see how successful that process has been in making nearly perfect (and wonderfully easy to use) *operational amplifiers*, and in Chapters 8–11 we'll see how digital electronics has been revolutionized by MOSFET integrated circuits. Because many FETs using very low current can be constructed in a small area, they are especially useful for large-scale integration (LSI) digital circuits such as calculator chips, microprocessors, and memories. In addition, high-current MOSFETs (30A or more) of recent design have been replacing bipolar transistors in many applications, often providing simpler circuits with improved performance.

3.01 FET characteristics

Beginners sometimes become catatonic when directly confronted with the confusing variety of FET types (see, for example, the first edition of this book!), a variety that arises from the combined choices of polarity (*n-channel* or *p-channel*), form of gate insulation (semiconductor *junction* [JFET] or oxide *insulator* [MOSFET]), and channel doping (*enhancement* or *depletion* mode). Of the eight resulting possibilities, six *could* be made, and five actually are. Four of those five are of major importance.

It will aid understanding (and sanity), however, if we begin with one type only, just as we did with the *npn* bipolar transistor. Once comfortable with FETs, we'll have little trouble with their family tree.

FET V–I curves

Let's look first at the *n*-channel enhancement-mode MOSFET, which is analogous to the *npn* bipolar transistor (Fig. 3.1). In normal operation the drain (~collector) is more positive than the source (~emitter). No current flows from drain to source unless the gate (~base) is brought positive with respect to the source. Once the gate is thus "forward-biased" there will be drain current, all of which flows to the source. Figure 3.2 shows how the drain current I_D varies with drain-source voltage V_{DS}, for a few values of controlling gate-source voltage V_{GS}. For comparison, the corresponding "family" of curves of I_C versus V_{BE} for an ordinary *npn* bipolar transistor is shown. Obviously threre are a lot of similarities between *n*-channel MOSFETs and *npn* bipolar transistors.

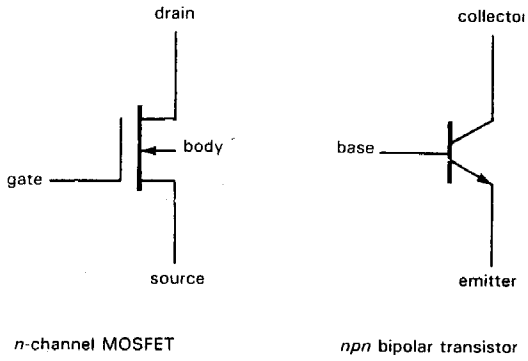


Figure 3.1

Like the *npn* transistor, the FET has a high incremental drain impedance, giving roughly constant current for V_{DS} greater than a volt or two. By an unfortunate choice of language, this is called the "saturation" region of the FET and corresponds to the "active" region of the bipolar transistor. Analogous to the bipolar transistor, larger gate-to-source bias produces larger drain current. If anything, FETs behave more nearly like ideal transconductance devices (constant drain current for constant gate-source voltage) than do bipolar

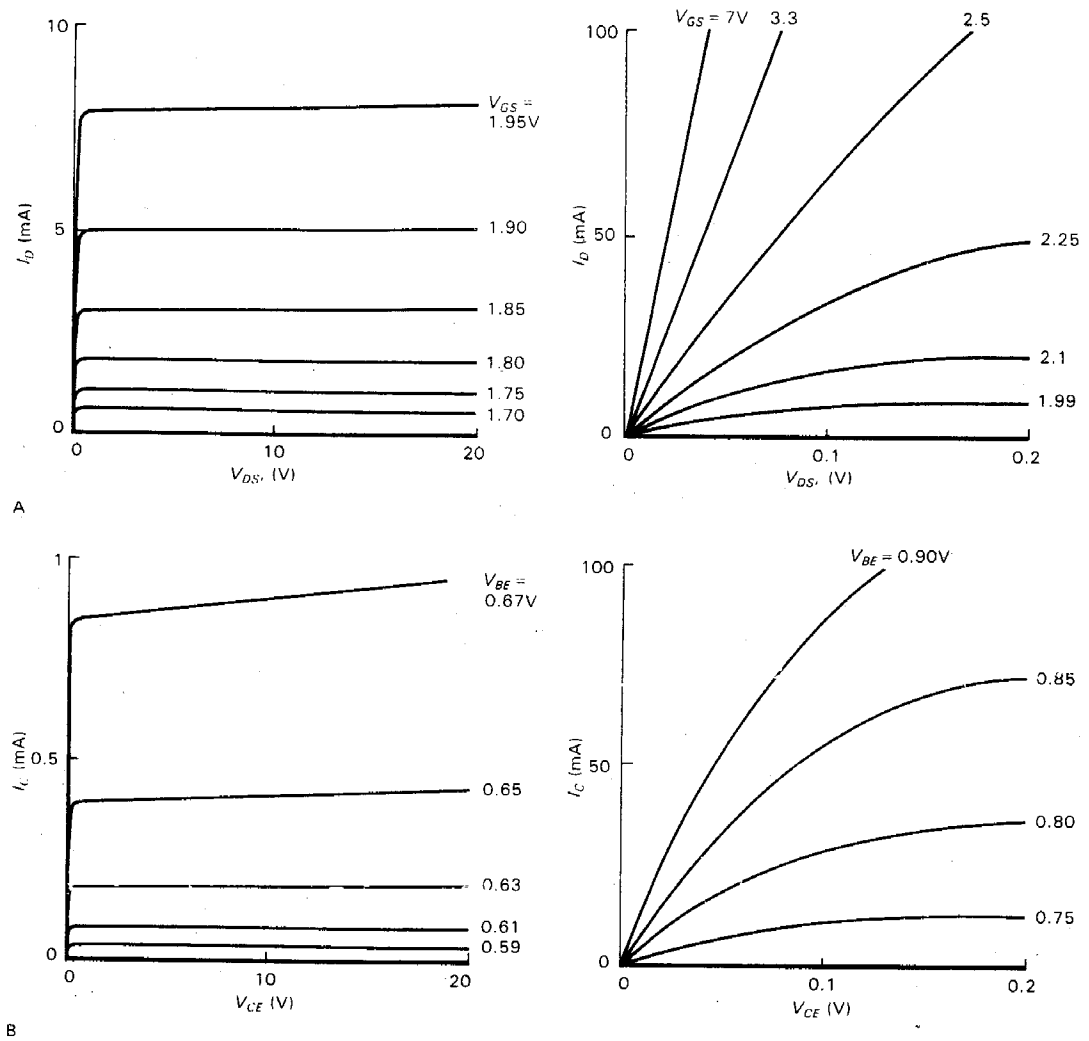


Figure 3.2. Measured MOSFET/transistor characteristic curves.
A. VN0106 n-channel MOSFET: I_D versus V_{DS} for various values of V_{GS}.
B. 2N3904 *npn* bipolar transistor: I_C versus V_{CE} for various values of V_{BE}.

transistors; the Ebers-Moll equation predicts perfect transconductance characteristics for bipolar transistors, but that ideal behavior is degraded by the Early effect (Section 2.10).

So far, the FET looks just like the *npn* transistor. Let's look closer, though. For one thing, over the normal range of currents the saturation drain current increases rather modestly with increasing gate voltage (V_{GS}). In fact, it is proportional to $(V_{GS} - V_T)^2$, where V_T is the "gate threshold voltage" at which drain current begins ($V_T \approx 1.63$V for the FET in Fig. 3.2); compare this mild quadratic law with the steep exponential transistor law, as given to us by Ebers and Moll. Second, there is *zero* dc gate current, so you mustn't think of the FET as a device with current gain (which would be infinite). Instead, think

of the FET as a transconductance device, with gate-source voltage programming the drain current, as we did with the bipolar transistor in the Ebers-Moll treatment; recall that the transconductance g_m is simply the ratio i_d/v_{gs} (recall the convention of using lower-case letters to indicate "small-signal" changes in a parameter; e.g., $i_d/v_{gs} = \delta I_d/\delta V_{gs}$). Third, the gate of a MOSFET is truly insulated from the drain-source channel; thus, unlike the situation for bipolar transistors (or JFETs, as we'll see), you can bring it positive (or negative) at least 10 volts or more without worrying about diode conduction. Finally, the FET differs from the bipolar transistor in the so-called linear region of the graph, where it behaves rather accurately like a resistor, *even for negative* V_{DS}; this turns out to be quite useful because the equivalent drain-source resistance is, as you might guess, programmed by the gate-source voltage.

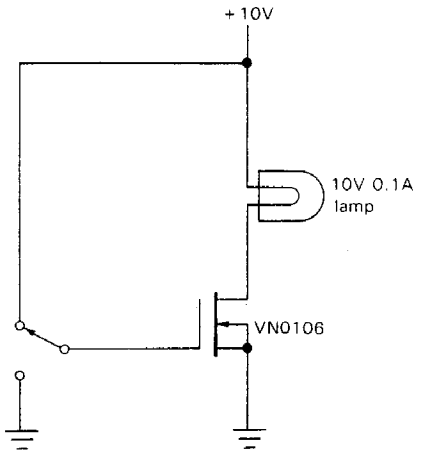


Figure 3.3. MOSFET switch.

Two examples

FETs have more surprises in store for us. Before getting into more details, though, let's look at two simple switching pplications. Figure 3.3 shows the MOSFET equivalent of Figure 2.3, our first saturated transistor switch. The FET circuit is even simpler, because we don't have to concern ourselves with the inevitable compromise of providing adequate base drive current (considering worst-case minimum h_{FE} combined with the lamp's cold resistance) without squandering excessive power. Instead, we just apply a full-swing dc voltage drive to the cooperative high-impedance gate. As long as the switched-on FET behaves like a resistance small compared with the load, it will bring its drain close to ground; typical power MOSFETs have $R_{ON} < 0.2$ ohm, which is fine for this job.

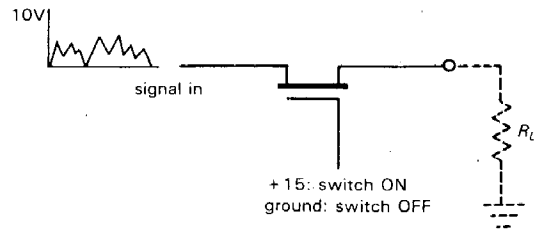


Figure 3.4

Figure 3.4 shows an "analog switch" application, which cannot be done at all with bipolar transistors. The idea here is to switch the conduction of a FET from open-circuit (gate reverse-biased) to short-circuit (gate forward-biased), thus blocking or passing the analog signal (we'll see plenty of reasons to do this sort of thing later). In this case we just arrange for the gate to be driven more negative than any input signal swing (switch *open*), or a few volts more positive than any input signal swing (switch *closed*). Bipolar transistors aren't suited to this application, because the base draws current and forms diodes with the emitter and collector, producing awkward clamping action. The MOSFET is delightfully simple by comparison, needing only a voltage swing into the (essentially open-circuit) gate. Warning:

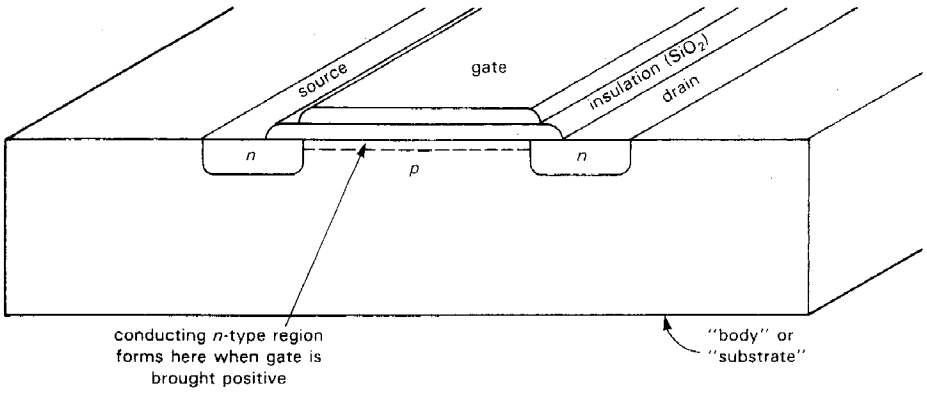


Figure 3.5. An n-channel MOSFET.

It's only fair to mention that our treatment of this circuit has been somewhat simplistic, for instance ignoring the effects of gate-channel capacitance and the variation of R_{ON} with signal swing. We'll have more to say about analog switches later.

3.02 FET types

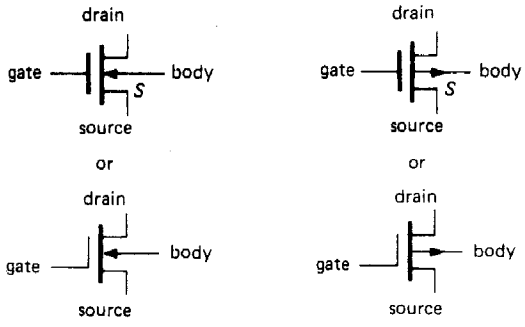
n-channel, p-channel

Now for the family tree. First of all, FETs (like BJTs) can be fabricated in both polarities. Thus, the mirror twin of our n-channel MOSFET is a *p-channel* MOSFET. Its behavior is symmetrical, mimicking *pnp* transistors: The drain is normally negative with respect to the source, and drain current flows if the gate is brought at least a volt or two negative with respect to the source. The symmetry isn't perfect because the carriers are holes, rather than electrons, with lower "mobility" and "minority carrier lifetime." These are semiconductor parameters of importance in transistor performance. The consequence is worth remembering – p-channel FETs usually have poorer performance, manifested as higher gate threshold voltage, higher R_{ON}, and lower saturation current.

MOSFET, JFET

In a MOSFET ("Metal-Oxide-Semiconductor Field-Effect Transistor") the gate region is separated from the conducting channel by a thin layer of SiO_2 (glass) grown onto the channel (Fig. 3.5). The gate, which may be either metal or doped silicon, is truly insulated from the source-drain circuit, with characteristic input resistance $>10^{14}$ ohms. It affects channel conduction purely by its electric field. MOSFETs are sometimes called *insulated-gate* FETs, or IGFETs. The gate insulating layer is quite thin, typically less than a wavelength of light, and can withstand gate voltages up to ± 20 volts or more. MOSFETs are easy to use because the gate can swing either polarity relative to the source without any gate current flowing. They are, however, quite susceptible to damage from static electricity; you can destroy a MOSFET device literally by touching it.

The symbols for MOSFETs are shown in Figure 3.6. The extra terminal is the "body," or "substrate," the piece of silicon in which the FET is fabricated (see Fig. 3.5). Because the body forms a diode junction with the channel, it must be held at a nonconducting voltage. It can be tied to the source, or to a point in the



A. n-channel MOSFET B. p-channel MOSFET

Figure 3.6

circuit more negative (positive) than the source for n-channel (p-channel) MOSFETs. It is common to see the body terminal omitted; furthermore, engineers often use the symbol with the symmetrical gate. Unfortunately, with what's left you can't tell source from drain; worse still, you can't tell n-channel from p-channel! We will use the lower set of schematic symbols exclusively in this book to avoid confusion, although we will often leave the body pin unconnected.

In a JFET ("Junction Field-Effect Transistor") the gate forms a semiconductor junction with the underlying channel. This has the important consequence that *a JFET gate should not be forward biased with respect to the channel, to prevent gate current.* For example, diode conduction will occur as the gate of an n-channel JFET approaches +0.6 volt with respect to the more negative end of the channel (which is usually the source). The gate is therefore operated reverse-biased with respect to the channel, and no current (except diode leakage) flows in the gate circuit. The circuit symbols for JFETs are shown in Figure 3.7. Once again, we favor the symbol with offset gate, to identify the source. As we'll see later, FETs (both JFET and MOSFET) are nearly symmetrical, but the gate-drain capacitance is usually designed to be less than the gate-source capacitance, making the drain the preferred output terminal.

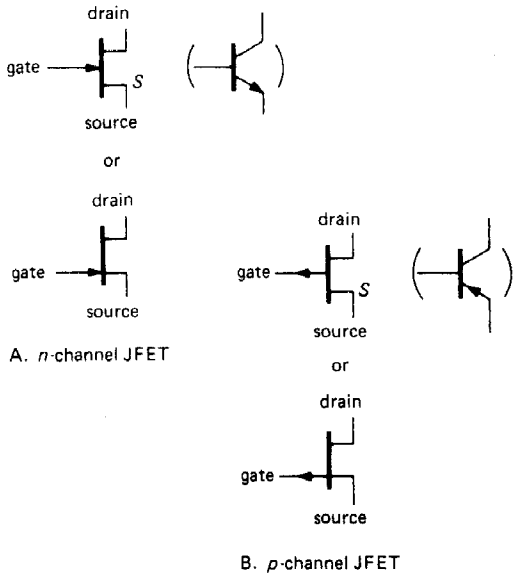


Figure 3.7

Enhancement, depletion

The n-channel MOSFETs with which we began the chapter were nonconducting, with zero (or negative) gate bias, and were driven into conduction by bringing the gate positive with respect to the source. This kind of FET is known as *enhancement mode.* The other possibility is to manufacture the n-channel FET with the channel semiconductor "doped" so that there is plenty of channel conduction even with zero gate bias, and the gate must be reverse-biased a few volts to cut off the drain current. Such a FET is known as *depletion mode.* MOSFETs can be made in either variety, since there is no restriction on gate polarity. But JFETs permit only reverse gate bias and therefore can be made only in depletion mode.

A graph of drain current versus gate-source voltage, at a fixed value of drain voltage, may help clarify this distinction (Fig. 3.8). The enhancement-mode device draws no drain current until the gate

is brought positive (these are n-channel FETs) with respect to the source, whereas the depletion-mode device is operating at nearly its maximum value of drain current when the gate is at the same voltage as the source. In some sense the two categories are artificial, because the two curves are identical except for a shift along the V_{GS} axis. In fact, it is possible to manufacture "in-between" MOSFETs. Nevertheless, the distinction is an important one when it comes to circuit design.

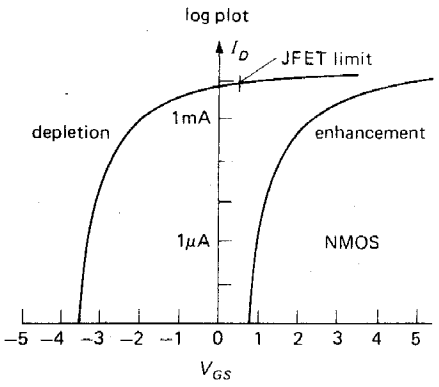


Figure 3.8

Note that JFETs are always depletion-mode devices and that the gate cannot be brought more than about 0.5 volt more positive (for n-channel) than the source, since the gate-channel diode will conduct. MOSFETs *could* be either enhancement or depletion, but in practice you rarely see depletion-mode MOSFETs (the exceptions being n-channel GaAs FETs and "dual-gate" cascodes for radiofrequency applications). For all practical purposes, then, you have to worry only about (a) depletion-mode JFETs and (b) enhancement-mode MOSFETs; they both come in the two polarities, n-channel and p-channel.

3.03 Universal FET characteristics

A family tree (Fig. 3.9) and a map (Fig. 3.10) of input/output voltage (source grounded) may help simplify things. The different devices (including garden-variety *npn* and *pnp* bipolar transistors) are drawn in the quadrant that characterizes their input and output voltages when they are in the active region with source (or emitter) grounded. You don't have to remember the properties of the five kinds of FETs, though, because they're all basically the same.

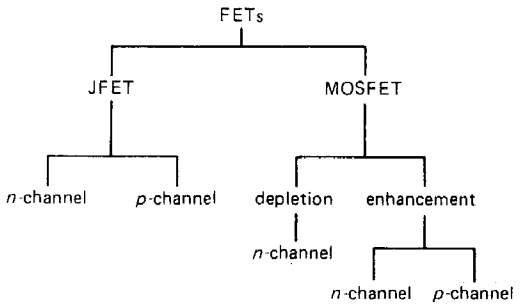


Figure 3.9

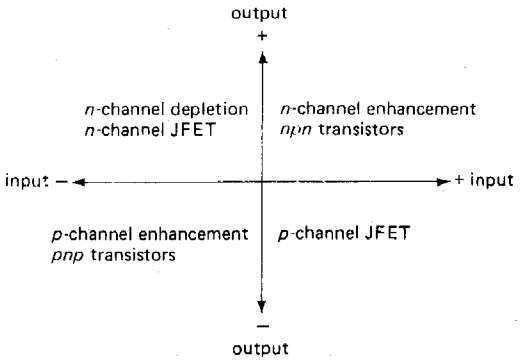


Figure 3.10

First, with the source grounded, a FET is turned on (brought into conduction) by bringing the gate voltage "toward" the active drain supply voltage. This is true for all five types of FETs, as well as the bipolar transistors. For example, an n-channel JFET (which is automatically depletion-mode) uses a positive drain supply, as do all n-type devices. Thus a positive-going gate voltage tends to turn on the JFET.

The subtlety for depletion-mode devices is that the gate must be (negatively) back-biased for zero drain current, whereas for enhancement-mode devices zero gate voltage is sufficient to give zero drain current.

Second, because of the near symmetry of source and drain, either terminal can act as the effective source (exception: not true for power MOSFETs, where the body is internally connected to the source). When thinking of FET action, and for purposes of calculation, the effective source terminal is always the one most "away" from the active drain supply. For example, suppose a FET is used to switch a line to ground, and both positive and negative signals are present on the switched line, which is usually selected to be the FET drain. If the switch is an n-channel MOSFET (therefore enhancement), and a negative voltage happens to be present on the (turned-off) drain terminal, then that terminal is actually the "source" for purposes of gate turn-on voltage calculation. Thus a negative gate voltage larger than the most negative signal, rather than ground, is needed to ensure turn-off.

The graph in Figure 3.11 may help you sort out all these confusing ideas. Again, the difference between enhancement and depletion is merely a question of displacement along the V_{GS} axis – i.e., whether there is a lot of drain current or no drain current at all when the gate is at the same potential as the source. The n-channel and p-channel FETs are complementary in the same way as *npn* and *pnp* bipolar transistors.

In Figure 3.11 we have used standard symbols for the important FET parameters of saturation current and cutoff voltage. For JFETs the value of drain current with gate shorted to source is specified on the data sheets as I_{DSS} and is nearly the maximum drain current possible. (I_{DSS} means current from *d*rain to *s*ource with the gate *s*horted to the source. Throughout the chapter you will see this notation, in which the first two subscripted letters designate the pair of terminals, and the third specifies the condition.) For enhancement-mode MOSFETs the analogous specification is $I_{D(ON)}$, given at some forward gate voltage ("I_{DSS}" would be zero for any enhancement-mode device).

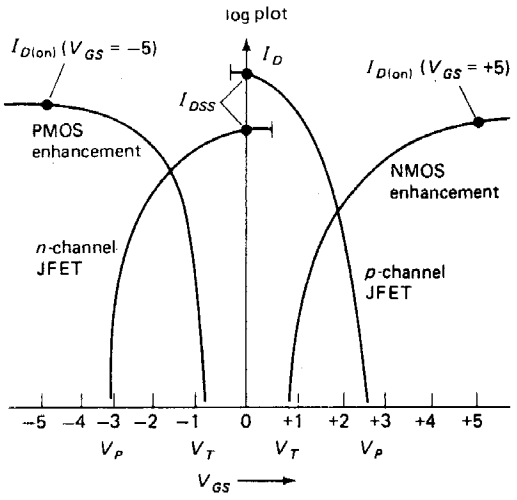


Figure 3.11

For JFETs the gate-source voltage at which drain current approaches zero is called the "gate-source cutoff voltage," $V_{GS(OFF)}$, or the "pinch-off voltage," V_P, and is typically in the range of −3 to −10 volts (positive for p-channel, of course). For enhancement-mode MOSFETs the analogous quantity is the "threshold voltage," V_T (or $V_{GS(th)}$), the gate-source voltage at which drain current begins to flow. V_T is typically in the range of 0.5 to 5 volts, in the "forward" direction, of course. Incidentally, don't confuse the MOSFET V_T with the V_T in the Ebers-Moll equation that describes bipolar transistor collector current; they have nothing to do with each other.

With FETs it is easy to get confused about polarities. For example, n-channel devices, which usually have the drain

positive with respect to the source, can have positive or negative gate voltage, and positive (enhancement) or negative (depletion) threshold voltages. To make matters worse, the drain can be (and often is) operated negative with respect to the source. Of course, all these statements go in reverse for p-channel devices. In order to minimize confusion, we will always assume n-channel devices unless explicitly stated otherwise. Likewise, because MOSFETs are nearly always enhancement-mode, and JFETs are always depletion-mode, we'll omit those designations from now on.

3.04 FET drain characteristics

In Figure 3.2 we showed a family of curves of I_D versus V_{DS} that we measured for a VN0106, an n-channel enhancement-mode MOSFET. (The VN01 comes in various voltage ratings, indicated by the last two digits of the part number. For example, a VN0106 is rated at 60V.) We remarked that FETs behave like pretty good transconductance devices over most of the graph (i.e., I_D nearly constant for a given V_{DS}), except at small V_{DS}, where they approximate a resistance (i.e., I_D proportional to V_{DS}). In both cases the applied gate-source voltage controls the behavior, which can be well described by the FET analog of the Ebers-Moll equation. Let's look at these two regions a bit more closely.

Figure 3.12 shows the situation schematically. In both regions the drain current depends on $V_{GS} - V_T$, the amount by which the applied gate-source voltage exceeds the threshold (or pinch-off) voltage. The linear region, in which drain current is approximately proportional to V_{DS}, extends up to a voltage $V_{DS(\text{sat})}$, after which the drain current is approximately constant. The slope in the linear region, I_D/V_{DS}, is proportional to the gate bias, $V_{GS} - V_T$. Furthermore, the drain voltage at which the curves enter the "saturation region," $V_{DS(\text{sat})}$, equals $V_{GS} - V_T$, making the saturation drain current, $I_{D(\text{sat})}$, proportional to $(V_{GS} - V_T)^2$, the quadratic law we mentioned earlier. For reference, here are the universal FET drain-current formulas:

$$I_D = 2k[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2] \quad \text{(linear region)}$$

$$I_D = k(V_{GS} - V_T)^2 \quad \text{(saturation region)}$$

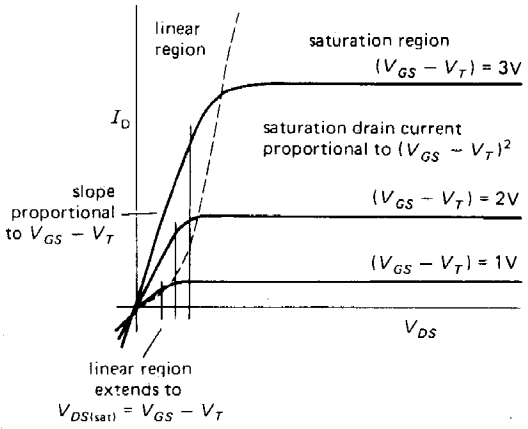


Figure 3.12

If we call $V_{GS} - V_T$ (the amount by which the gate-source voltage exceeds the threshold) the "gate drive," the important results are that (a) the resistance in the linear region is inversely proportional to gate drive, (b) the linear region extends to a voltage equal to the gate drive, and (c) saturation drain current is proportional to the square of the gate drive. These equations assume that the body is connected to the source. Note that the "linear region" is not really linear, because of the V_{DS}^2 term; we'll show a clever circuit fix later.

The scale factor k depends on particulars such as the geometry of the FET, oxide capacitance, and carrier mobility. It has a temperature dependence $k \propto T^{-3/2}$, which alone would cause I_D to decrease

with increasing temperature. However, V_T also depends slightly on temperature (2–5mV/°C); the combined effect produces the curve of drain current versus temperature shown in Figure 3.13.

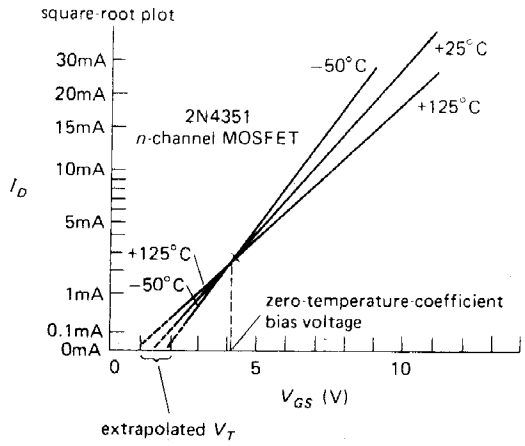


Figure 3.13

At large drain currents the negative temperature coefficient of k causes the drain current to decrease with increasing temperature – goodbye thermal runaway! As a consequence, FETs of a given type can be paralleled without the external current-equalizing ("emitter-ballasting") resistors that you must use with bipolar transistors (see Section 6.07). This same negative coefficient also prevents thermal runaway in local regions of the junction (an effect known as "current hogging"), which severely limits the power capability of large bipolar transistors, as we'll see when we discuss "second breakdown" and "safe operating area" in Chapter 6.

At small drain currents (where the temperature coefficient of V_T dominates), I_D has a positive tempco, with a point of zero temperature coefficient at some drain current in between. This effect is exploited in FET op-amps to minimize temperature drift, as we'll see in the next chapter.

Subthreshold region

Our expression given earlier for saturation drain current does not apply for very small drain currents. This is known as the "subthreshold" region, where the channel is below the threshold for conduction, but some current flows anyway because of a small population of thermally energetic electrons. If you've studied physics or chemistry, you probably know in your bones that the resulting current is exponential:

$$I_D = k \exp(V_{GS} - V_T)$$

We measured some MOSFETs over 9 decades of drain current (1nA to 1A) and plotted the result as a graph of I_D versus V_{GS} (Fig. 3.14). The region from 1nA to 1mA is quite precisely exponential; above this subthreshold region the curves enter the normal saturation region. For the n-channel MOSFET (type VN01) we checked out a sample of 20 transistors (from four different manufacturing runs spread over 2 years), plotting the extreme range to give you an idea of the variability (see next section). Note the somewhat poorer characteristics (V_T, $I_{D(ON)}$) of the "complementary" VP01.

3.05 Manufacturing spread of FET characteristics

Before we look at some circuits, let's take a look at the range of FET parameters (such as I_{DSS} and V_T), as well as their manufacturing "spread" among devices of the same nominal type, in order to get a better idea of the FET. Unfortunately, many of the characteristics of FETs show much greater process spread than the corresponding characteristics of bipolar transistors, a fact that the designer must keep in mind. For example, the VN01 (a typical n-channel MOSFET) has a specified V_T of 0.8 to 2.4 volts (I_D = 1mA), compared with the analogous V_{BE} spread of

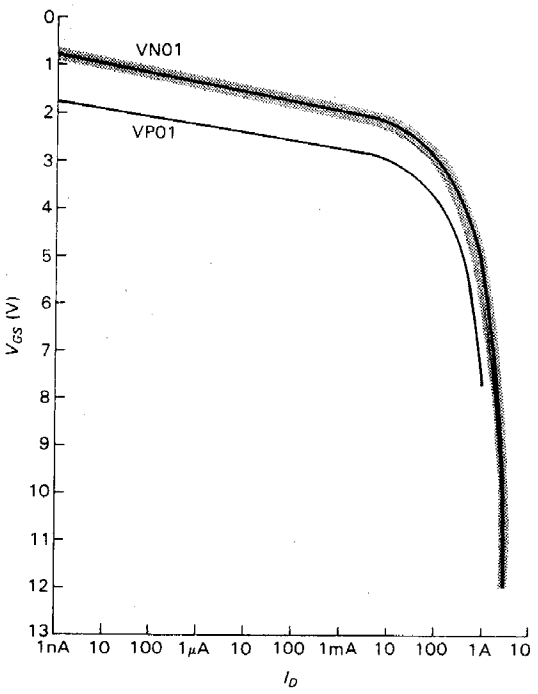


Figure 3.14. Measured MOSFET drain current versus gate-source voltage.

0.63 to 0.33 volt (also at I_C = 1mA) for an *npn* bipolar transistor. Here's what you can expect:

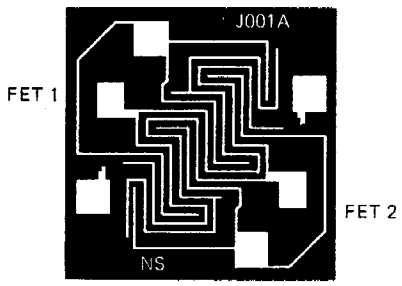
Characteristic	*Available range*	*Spread*
I_{DSS}, $I_{D(ON)}$	1mA to 100A	×5
$R_{DS(ON)}$	0.05Ω to 10k	×5
g_m @ 1mA	500–3000μS	×5
V_P (JFETs)	0.5–10V	5V
V_T (MOSFETs)	0.5–5V	2V
$BV_{DS(OFF)}$	6–1000V	
$BV_{GS(OFF)}$	6–125V	

$R_{D(ON)}$ is the drain-source resistance (linear region, i.e., small V_{DS}) when the FET is conducting fully, e.g., with the gate grounded in the case of JFETs or with a large applied gate-source voltage (usually specified as 10V) for MOSFETs. I_{DSS} and $I_{D(ON)}$ are the saturation-region (large V_{DS}) drain currents under the same turned-on gate drive conditions. V_P is the pinch-off voltage (JFETs), V_T is the turn-on gate threshold voltage (MOSFETs), and the BVs are breakdown voltages. As you can see, a JFET with grounded source may be a good current source, but you can't predict very well what the current will be. Likewise, the V_{GS} needed to produce some value of drain current can vary considerably, in contrast to the predictable (≈0.6V) V_{BE} of bipolar transistors.

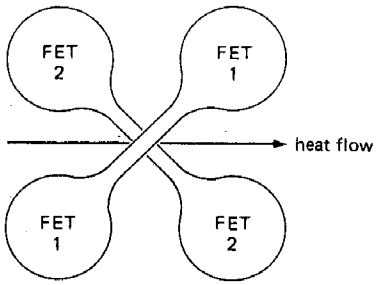
Matching of characteristics

As you can see, FETs are inferior to bipolar transistors in V_{GS} predictability, i.e., they have a large spread in the V_{GS} required to produce a given I_D. Devices with a large process spread will, in general, have larger offset (voltage unbalance) when used as differential pairs. For instance, typical run-of-the-mill bipolar transistors might show a spread in V_{BE} of 50mV or so, at some collector current, for a selection of off-the-shelf transistors. The comparable figure for MOSFETs is more like 1 volt! Because FETs have some very desirable characteristics otherwise, it is worthwhile putting in some extra effort to reduce these offsets in specially manufactured matched pairs. IC designers use techniques like interdigitation (two devices sharing the same general piece of IC real estate) and thermal-gradient cancellation schemes to improve performance (Fig. 3.15).

The results are impressive. Although FET devices still cannot equal bipolar transistors in V_{GS} matching, their performance is adequate for most applications. For example, the best available matched FET has a voltage offset of 0.5mV and tempco of 5μV/°C (max), whereas the best bipolar pair has values of 25μV and 0.6μV/°C (max), roughly 10 times better. Operational amplifiers (the universal high-gain differential amplifiers we'll see in the next chapter) are available in both flavors; you would generally choose one with bipolar innards for high precision (because of its



A. interdigitation



B. temperature-gradient cancellation

Figure 3.15

close input-transistor V_{BE} matching), whereas a FET-input op-amp is the obvious choice for high-impedance applications (because its inputs – FET gates – draw no current). For example, the inexpensive JFET-input LF411 that we will use as our all-around op-amp in the next chapter has a typical input current of 50pA and costs $0.60; the popular MOSFET-input TLC272 costs about the same and has a typical input current of only 1pA! Compare this with a common bipolar op-amp, the μA741, with typical input current of 80,000pA (80nA).

Tables 3.1–3.3 list a selection of typical JFETs (both single and dual) and small-signal MOSFETs. Power MOSFETs, which we will discuss in Section 3.14, are listed in Table 3.5.

BASIC FET CIRCUITS

Now we're ready to look at FET circuits. You can usually find a way to convert a circuit that uses BJTs into one using FETs. However, the new circuit may not be an improvement! For the remainder of the chapter we'd like to illustrate circuit situations that take advantage of the unique properties of FETs, i.e., circuits that work better with FETs, or that you can't build at all with bipolar transistors. For this purpose it may be helpful to group FET applications into categories; here are the most important, as we see it:

High-impedance/low-current. Buffers or amplifiers for applications where the base current and finite input impedance of BJTs limit performance. Although you *can* build such circuits with discrete FETs, current practice favors using integrated circuits built with FETs. Some of these use FETs as a high-impedance front-end for an otherwise bipolar design, whereas others use FETs throughout.

Analog switches. MOSFETs are excellent voltage-controlled analog switches, as we hinted in Section 3.01. We'll look briefly at this subject. Once again, you should generally use dedicated "analog switch" ICs, rather than building discrete circuits.

Digital logic. MOSFETs dominate microprocessors, memory, and most high-performance digital logic. They are used exclusively in micropower logic. Here, too, MOSFETs make their appearance in integrated circuits. We'll see why FETs are preferable to BJTs.

Power switching. Power MOSFETs are often preferable to ordinary bipolar power transistors for switching loads, as we suggested in our first circuit of the chapter. For this application you use *discrete* power FETs.

Variable resistors; current sources. In the "linear" region of the drain curves, FETs behave like voltage-controlled resistors; in the "saturation" region they are voltage-controlled current sources. You can exploit this intrinsic behavior of FETs in your circuits.

TABLE 3.1. JFETs

Type	BV_{GSS} (V)	I_{DSS} min (mA)	I_{DSS} max (mA)	$V_{GS(OFF)}, V_P$ min (V)	$V_{GS(OFF)}, V_P$ max (V)	max (pF)	max (pF)	Comments
n-channel								
2N4117A-	40	0.03	0.09	0.6	1.8	3	1.5	low leakage: 1pA (max)
2N4119A	40	0.24	0.6	2	6	4	1.5	
2N4338	50	0.2	0.6	0.3	1	6	2	0.5fA/√Hz @ 100Hz
2N4416	30	5	15	2.5	6	4	0.8	VHF low noise: <2dB@100MHz
2N4867A-	40	0.4	1.2	0.7	2	25	5	low freq, low noise:
2N4869A	40	2.5	7.5	1.8	5	25	5	10nV/√Hz(max)@10Hz
2N5265-	60	0.5	1	–	3	7	2	series of 6, tight I_{DSS} spec;
2N5270	60	7	14	–	8	7	2	2N5358-64 p-chan complement
2N5432	25	150	–	4	10	30	15	switch: R_{ON}=5Ω(max)
2N5457-	25	1	5	0.5	6	7	3	general purpose;
2N5459	25	4	16	2	8	7	3	2N5460-2 p-chan complement
2N5484-	25	1	5	0.3	3	5	1	low noise RF; inexpensive
2N5486	25	8	20	2	6	5	1	
2SK117	50	0.6	14	0.2	1.5	13[t]	3[t]	ultra low noise: 1nV/√Hz
2SK147	40	5	30	0.3	1.2	75[t]	15[t]	ultra low noise: 0.7nV/√Hz
p-channel								
2N5114	30	30	90	5	10	25	7	switch: R_{ON}=75Ω(max)
2N5358-	40	0.5	1	0.5	3	6	2	series of 7, tight I_{DSS} spec;
2N5364	40	9	18	2.5	8	6	2	2N5265-70 n-chan complement
2N5460-	40	1	5	0.75	6	7	2	general purpose;
2N5462	40	4	16	1.8	9	7	2	2N5457-9 n-chan complement
2SJ72	25	5	30	0.3	2	185[t]	55[t]	ultra low noise: 0.7nV/√Hz

[t] typical.

Generalized replacement for bipolar transistors. You can use FETs in oscillators, amplifiers, voltage regulators, and radio-frequency circuits (to name a few), where bipolar transistors are also normally used. FETs aren't *guaranteed* to make a better circuit – sometimes they will, sometimes they won't. You should keep them in mind as an alternative.

Now let's look at these subjects. We'll adopt a slightly different order, for clarity.

3.06 JFET current sources

JFETs are used as current sources within integrated circuits (particularly op-amps), and also sometimes in discrete designs. The simplest JFET current source is shown in Figure 3.16; we chose a JFET, rather than a MOSFET, because it needs no gate bias (it's depletion mode). From a graph of FET drain characteristics (Fig. 3.17) you can see that the current will be reasonably

TABLE 3.2. SELECTED MOSFETs

Type	Mfg[a]	Gate protec	$R_{DS(on)}$ max @V_{GS} (Ω)	(V)	$V_{GS(th)}$ min (V)	max (V)	$I_{D(on)}$ (V_{DS}=10V) min (mA)	C_{rss} max (pF)	BV_{DS} (V)	BV_{GS} (V)	I_{GSS} (nA)	Comments
n-channel												
3SK38A	TO	•	500	3	–	–	10	2.5	20	12	25	
3N170	IL	–	200	10	1.0	2	10	1.3	25	35	0.01	
SD210	SI	–	45	10	0.5	2	–	0.5	30	40	0.1	low R_{ON}
SD211	SI	•	45	10	0.5	2	–	0.5	30	15	10	low R_{ON}
VN1310	ST	–	8	10	0.8	2.4	500	5	100	20	0.1	small VMOS; D-S diode
IT1750	IL	–	50	20	0.5	3	10	1.6	25	25	0.01	
VN2222L	SI	–	8	5	0.6	2.5	750	5	60	40	0.1	small VMOS; D-S diode
CD3600	RC	•	500	10	1.5[t]	–	1.3	0.4	15	15	0.01	equiv to 4007 array
2N3796	MO	–	–	–	-4	–	14	0.8	25	10	0.001	depletion; I_{DSS}=1.5mA
2N4351	MO+	–	300	10	1.5	5	3	2.5	25	35	0.01	popular
p-channel												
3N163	IL	–	250	20	2	5	5	0.7	40	40	0.01	
VP1310	ST	–	25	10	1.5	3.5	250	5	100	20	0.1	small VMOS; D-S diode
IT1700	IL	–	400	10	2	5	2	1.2	40	40	0.01	
CD3600	RC	•	500	10	1.8[t]	–	1.3	0.8	15	15	0.02	equiv to 4007 array
2N4352	MO+	–	600	10	1.5	6	2	2.5	25	35	0.01	popular
3N172	IL	•	250	20	2	5	5	1	40	40	0.2	popular

[a] see footnotes to Table 4.1. [t] typical.

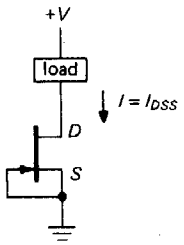


Figure 3.16

constant for V_{DS} larger than a couple of volts. However, because of I_{DSS} spread, the current is unpredictable. For example, the 2N5484 (a typical *n*-channel JFET) has a specified I_{DSS} of 1mA to 5mA. Still, the circuit is attractive because of the simplicity of a two-terminal constant-current device. If that appeals to you, you're in luck. You can buy "current-regulator diodes" that are nothing more than JFETs with gate tied to source, sorted according to current. They're the current analog of a zener (voltage regulator) diode. Here are the characteristics of the 1N5283–1N5314 series:

Currents available	0.22mA to 4.7mA
Tolerance	10%
Temperature coefficient	±0.4%/°C
Voltage range	1V–2.5V min, 100V max
Current regulation	5% typical
Impedance	1M typical (for 1mA device)

We plotted I versus V for a 1N5294 (rated at 0.75mA); Figure 3.18A shows

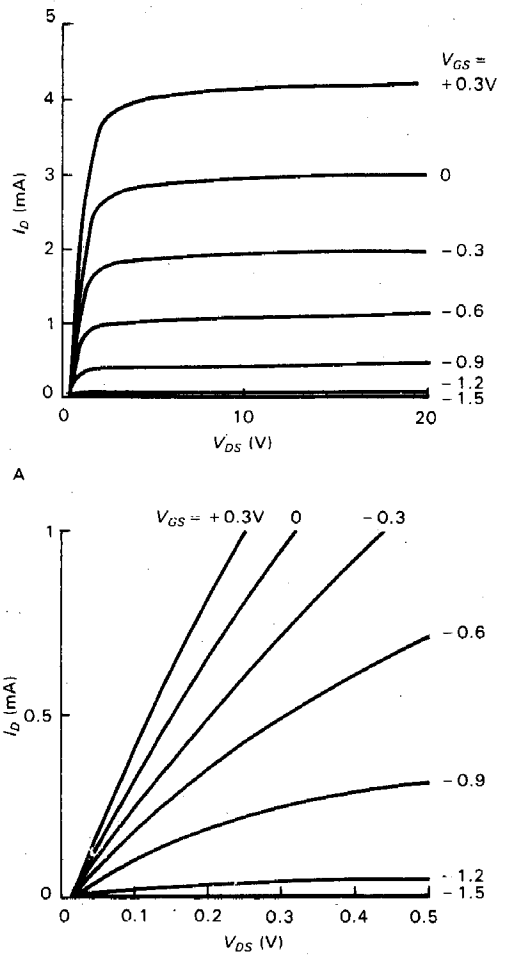


Figure 3.17. Measured JFET characteristic curves. 2N5484 n-channel JFET: I_D versus V_{DS} for various values of V_{GS}.

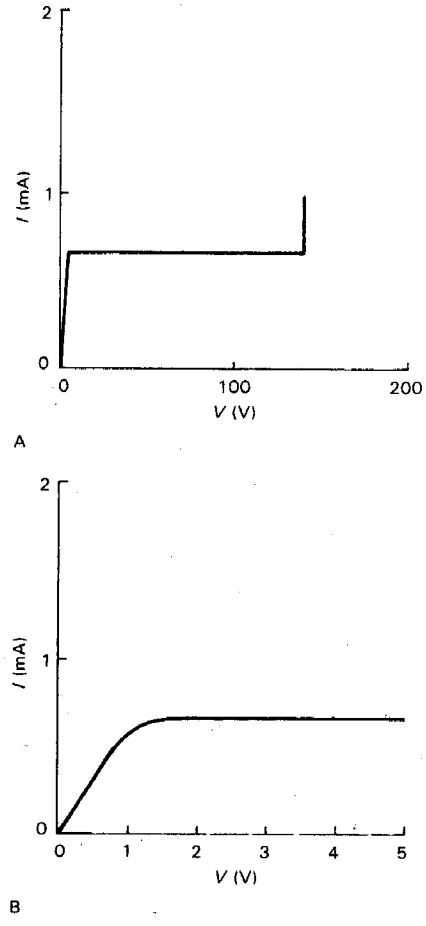


Figure 3.18. 1N5294 "current regulator diode."

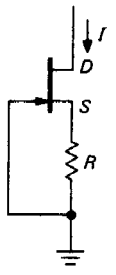


Figure 3.19

good constancy of current up to the breakdown voltage (140V for this particular specimen), whereas Figure 3.18B shows that the device reaches full current with somewhat less than 1.5 volts across it. We'll show how to use these devices to make a cute triangle-wave generator in Section 5.13. Table 3.4 is a partial listing of the 1N5283 series.

Source self-biasing

A variation of the previous circuit (Fig. 3.19) gives you an adjustable current source. The self-biasing resistor R back-biases the gate by $I_D R$, reducing I_D and bringing the JFET closer to pinch-off. You can calculate R from the drain curves for the particular JFET. This circuit allows you

TABLE 3.3. DUAL MATCHED n-CHANNEL JFETs

Type	V_{os} max (mV)	Drift max (μV/°C)	I_{GSS} (V_{DG}=20V) max (pA)	CMRR min (dB)	$V_{GS(OFF)}$, V_P min (V)	$V_{GS(OFF)}$, V_P max (V)	e_n (10Hz) max (nV/√Hz)	C_{rss} (V_{DG}=10V) max (pF)	Comments
U421	10	10	0.2	90	0.4	2	50	1.5	Siliconix
2N3954A	5	5	100	–	1	3	150[a]	1.2	gen purp, low drift
2N3955	5	25	100	–	1	4.5	150[a]	1.2	popular
2N3958	25	–	100	–	1	4.5	150[a]	1.2	
2N5196	5	5	15	–	0.7	4	20[b]	2	
2N5520	5	5	100	100	0.7	4	15	5	
2N5906	5	5	2	90[t]	0.6	4.5	70[t]	1.5	low gate leakage
2N5911	10	20	100	–	1	5	20[c]	1.2	low noise at high freq
2N6483	5	5	100	100	0.7	4	10	3.5	low noise at low freq
NDF9406	5	5	5	120	0.5	4	30	0.1	cascode: low C_{rss}
2N5452	5	5	100[d]	–	1	4.5	20[b]	1.2[e]	
2SK146	20	–	1000[d]	–	0.3	1.2	1.3	15[t]	ultra low noise

[a] at 100Hz. [b] at 1kHz. [c] at 10kHz. [d] at 30V. [e] at 20V. [t] typical.

to set the current (which must be less than I_{DSS}), as well as to make it more predictable. Furthermore, the circuit is a better current source (higher impedance) because the source resistor provides "current-sensing feedback" (which we'll learn about in Section 4.07), and also because FETs tend to be better current sources anyway when the gate is back-biased (as can perhaps be seen from the flatness of the lower drain-current curves in Figs. 3.2 and 3.17). Remember, though, that actual curves of I_D for some value of V_{GS} obtained with a real FET may differ markedly from the values read from a set of published curves, owing to manufacturing spread. You may therefore want to use an adjustable source resistor, if it is important to have a specific current.

EXERCISE 3.1

Use the 2N5484 measured curves in Figure 3.17 to design a JFET current source to deliver 1mA. Now ponder the fact that the specified I_{DSS} of a 2N5484 is 1mA (min), 5mA (max).

A JFET current source, even if built with source resistor, shows some variation of output current with output voltage; i.e., it has finite output impedance, rather than the desirable infinite Z_{out}. The measured curves of Figure 3.17, for example, suggest that over a drain voltage range of 5 to 20 volts, a 2N5484 shows a drain current variation of 5% when operated with gate tied to source (i.e., I_{DSS}). This might drop to 2% or so if you use a source resistor. The same trick used in Figure 2.24 can be used with JFET current sources and is shown in Figure 3.20. The idea (as with BJTs) is to use a second JFET to hold constant the drain-source voltage of the current source. Q_1 is an ordinary JFET current source, shown in this case with a source resistor. Q_2 is a JFET of larger I_{DSS}, connected "in series" with the current source. It passes Q_1's (constant) drain current through to the load, while holding Q_1's drain at a fixed voltage – namely the gate-source voltage that makes Q_2 operate at the same current as Q_1. Thus Q_2 shields Q_1 from voltage swings

TABLE 3.4. CURRENT-REGULATOR DIODES[a]

Type	I_P (mA)	Impedance (25V) min (MΩ)	V_{min} ($I > 0.8\ I_P$) (V)
1N5283	0.22	25	1.0
1N5285	0.27	14	1.0
1N5287	0.33	6.6	1.0
1N5288	0.39	4.1	1.1
1N5290	0.47	2.7	1.1
1N5291	0.56	1.9	1.1
1N5293	0.68	1.4	1.2
1N5294	0.75	1.2	1.2
1N5295	0.82	1.0	1.3
1N5296	0.91	0.9	1.3
1N5297	1.0	0.8	1.4
1N5299	1.2	0.6	1.5
1N5302	1.5	0.5	1.6
1N5304	1.8	0.4	1.8
1N5305	2.0	0.4	1.9
1N5306	2.2	0.4	2.0
1N5308	2.7	0.3	2.2
1N5309	3.0	0.3	2.3
1N5310	3.3	0.3	2.4
1N5312	3.9	0.3	2.6
1N5314	4.7	0.2	2.9

[a] all operate to 100V and 600mW, and look like diodes in the reverse direction

at its output; since Q_1 doesn't see drain voltage variations, it just sits there and provides constant current. If you look back at the Wilson mirror (Fig. 2.48), you'll see that it uses this same voltage clamping idea.

You may recognize this JFET circuit as the "cascode," which is normally used to circumvent Miller effect (Section 2.19). A JFET cascode is simpler than a BJT cascode, however, because you don't need a bias voltage for the gate of the upper FET: Because it's depletion-mode, you can simply ground the upper gate (compare with Fig. 2.74).

EXERCISE 3.2

Explain why the upper JFET in a cascode must have higher I_{DSS} than the lower JFET. It may help to consider a JFET cascode with no source resistor.

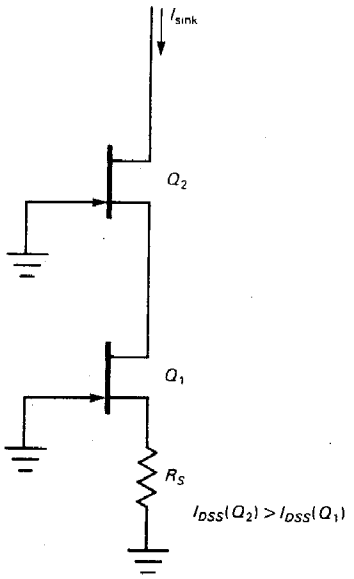


Figure 3.20. Cascode JFET current sink.

It is important to realize that a good bipolar transistor current source will give far better predictability and stability than a JFET current source. Furthermore, the op-amp-assisted current sources we'll see in the next chapter are better still. For example, a FET current source might vary 5% over a typical temperature range and load voltage variation, even after being set to the desired current by trimming the source resistor, whereas an op-amp/transistor (or op-amp/FET) current source is predictable and stable to better than 0.5% without great effort.

3.07 FET amplifiers

Source followers and common-source FET amplifiers are analogous to the emitter followers and common-emitter amplifiers made with bipolar transistors that we talked about in the last chapter. However, the absence of dc gate current makes

it possible to realize very high input impedances. Such amplifiers are essential when dealing with the high-impedance signal sources encountered in measurement and instrumentation. For some specialized applications you may want to build followers or amplifiers with discrete FETs; most of the time, however, you can take advantage of FET-input op-amps. In either case it's worth knowing how they work.

With JFETs it is convenient to use the same self-biasing scheme as with JFET current sources (Section 3.06), with a single gate-biasing resistor to ground (Fig. 3.21); MOSFETs require a divider from the drain supply, or split supplies, just as we used with BJTs. The gate-biasing resistors can be quite large (a megohm or more), because the gate leakage current is measured in nanoamps.

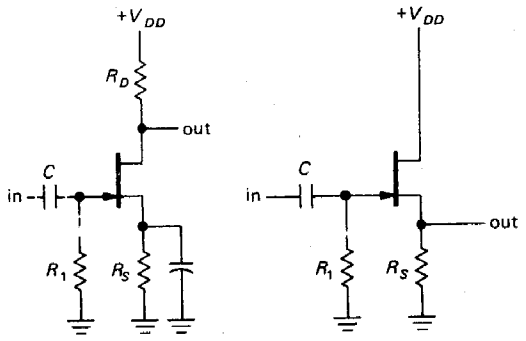


Figure 3.21

Transconductance

The absence of gate current makes *transconductance* (the ratio of output current to input voltage: $g_m = i_{out}/v_{in}$) the natural gain parameter for FETs. This is in contrast to bipolar transistors in the last chapter, where we at first flirted with the idea of current gain (i_{out}/i_{in}), then introduced the transconductance-oriented Ebers-Moll model: It's useful to think of BJTs either way, depending on the application.

FET transconductance can be estimated from the characteristic curves, either by looking at the increase in I_D from one gate-voltage curve to the next on the family of curves (Fig. 3.2 or 3.17), or, more simply, from the slope of the I_D–V_{GS} "transfer characteristics" curve (Fig. 3.14). The transconductance depends on drain current (we'll see how, shortly) and is, of course,

$$g_m(I_D) = i_d/v_{gs}$$

(Remember that lower-case letters indicate quantities that are small-signal variations.) From this we get the voltage gain

$$G_{\text{voltage}} = v_d/v_{gs} = -R_D i_d/v_{gs}$$
$$= -g_m R_D$$

just the same as the bipolar transistor result in Section 2.09, with load resistor R_C replaced by R_D. Typically, FETs have transconductances of a few thousand microsiemens (micromhos) at a few milliamps. Because g_m depends on drain current, there will be some variation of gain (nonlinearity) over the waveform as the drain current varies, just as we have with grounded emitter amplifiers (where $g_m = 1/r_e$, proportional to I_C). Furthermore, FETs in general have considerably lower transconductance than bipolar transistors, which makes them less suitable as amplifiers and followers. Let's look at this a little further.

Transconductance of FETs versus BJTs

To make our last remark quantitative, consider a JFET and a BJT, each operating at 1mA. Imagine they are connected as common source (emitter) amplifiers, with a drain (collector) resistor of 5k to a +10 volt supply (Fig. 3.22). Let's ignore details of biasing and concentrate on the gain. The BJT has an r_e of 25 ohms, hence a g_m of 40 mS, for a voltage gain of −200 (which you could have calculated directly as $-R_C/r_e$). A typical JFET (e.g., a

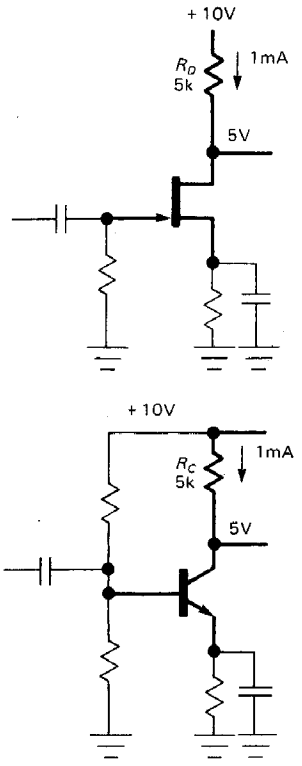


Figure 3.22

2N4220) has a g_m of 2mS at a drain current of 1mA, giving a voltage gain of -10. This seems discouraging by comparison. The low g_m also produces a relatively large Z_{out} in a follower configuration (Fig. 3.23): The JFET has

$$Z_{\text{out}} = 1/g_m$$

which in this case equals 500 ohms (independent of signal source impedance), to be compared with the BJT, which has

$$Z_{\text{out}} = R_s/h_{fe} + r_e = R_s/h_{fe} + 1/g_m$$

equal to R_s/h_{fe}+ 25 ohms (at 1mA). For typical transistor betas, say $h_{fe} = 100$, and reasonable signal sources, say with $R_s < 5k$, the BJT follower is an order of magnitude stiffer ($Z_{\text{out}} = 25\Omega$ to 75Ω). Note, however, that for $R_s > 50$k the JFET follower will be better.

To see what is happening, let's look back at the expressions for FET drain current versus gate-source voltage and compare with the equivalent expression (Ebers-Moll) for BJT collector current versus base-emitter voltage.

BJT: The Ebers-Moll equation,

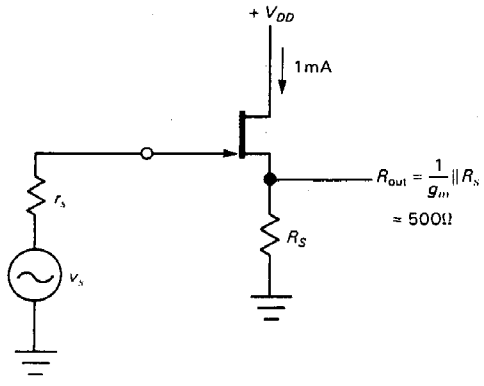
$$I_C = I_S\{\exp(V_{BE}/V_T) - 1\},$$
$$\text{with } V_T = kT/q = 25\,\text{mV}$$

predicts $g_m = dI_C/dV_{BE} = I_C/V_T$ for collector currents large compared with "leakage" current I_S. This is our familiar result $r_e(\text{ohms}) = 25/I_C(\text{mA})$, since $g_m = 1/r_e$.

FET: In the "subthreshold" region of very low drain current,

$$I_D \propto \exp(V_{GS})$$

which, being exponential like Ebers-Moll, also gives a transconductance proportional



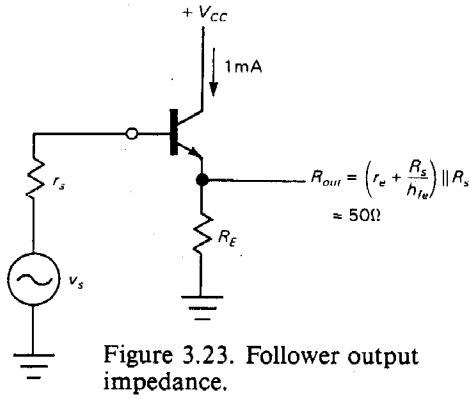


Figure 3.23. Follower output impedance.

to current. However, for real-world values of k (which is determined by FET geometry, carrier mobility, etc.) the FET's transconductance is somewhat lower than the BJT's, about $I/40\text{mV}$ for p-channel MOSFETs and $I/60\text{mV}$ for n-channel MOSFETs, as compared with $I/25\text{mV}$ for BJTs. As the current is increased, the FET enters the normal "saturation" region, where

$$I_D = k(V_{GS} - V_T)^2$$

which gives $g_m = 2(kI_D)^{1/2}$. That is, the transconductance increases only as the square root of I_D and is well below the transconductance of a bipolar transistor at the same operating current; see Figure 3.24. Increasing the constant k in our preceding equations (by raising the width/length ratio of the channel) increases the transconductance (and the drain current, for a given V_{GS}) in the region above threshold, but the transconductance still remains less than that of a bipolar transistor at the same current.

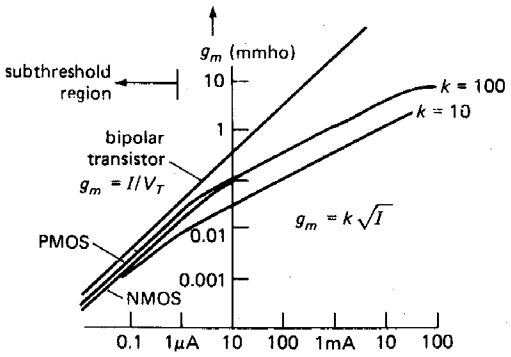


Figure 3.24. Comparison of g_m for bipolar transistors and FETs.

EXERCISE 3.3

Derive the foregoing expressions for g_m by differentiating I_{out} with respect to V_{in}.

The problem of low voltage gain in FET amplifiers can be circumvented by resorting to a current-source (active) load, but once again the bipolar transistor will be better in the same circuit. For this reason you seldom see FETs used as simple amplifiers, unless it's important to take advantage of their unique input properties (extremely high input resistance and low input current).

Note that FET transconductance in the saturation region is proportional to $V_{GS} - V_T$; thus, for example, a JFET with gate operated halfway to pinch-off has a transconductance approximately half that shown on the data sheet (where it is always given for $I_D = I_{DSS}$, i.e., $V_{GS} = 0$).

Differential amplifiers

Matched FETs can be used to construct high-input-impedance front-end stages for bipolar differential amplifiers, as well as the important op-amps and comparators we'll meet in the next chapter. As we mentioned earlier, the substantial V_{GS} offsets of FETs will generally result in larger input voltage offsets and offset drifts than with a comparable amplifier constructed entirely with bipolar transistors, but of course the input impedance will be raised enormously.

Oscillators

In general, FETs have characteristics that make them useful substitutes for bipolar transistors in almost any circuit that can benefit from their uniquely high input impedance and low bias current. A particular instance is their use in high-stability LC and crystal oscillators; we'll show examples in Sections 5.18, 5.19, and 13.11.

Active load

Just as with BJT amplifiers, it is possible to replace the drain-load resistor in a FET amplifier with an active load, i.e., a current

source. The voltage gain you get that way can be very large:

$$G_V = -g_m R_D$$

(with a drain resistor as load)

$$G_V = -g_m R_0$$

(with a current source as load)

where R_0 is the impedance looking into the drain (called "g_{oss}"), typically in the range of 100k to 1M.

One possibility for an active load is a current mirror as the drain load for a differential FET pair (see Section 2.18); the circuit is not bias-stable, however, without overall feedback. The current mirror can be constructed with either FETs or BJTs. This configuration is often used in FET op-amps, as we'll see in the next chapter. You will see another nice example of the active load technique in Section 3.14 when we discuss the CMOS linear amplifier.

3.08 Source followers

Because of the relatively low transconductance of FETs, it's often better to use a FET "source follower" (analogous to an emitter follower) as an input buffer to a conventional BJT amplifier, rather than trying to make a common-source FET amplifier directly. You still get the high input impedance and zero dc input current of the FET, and the BJT's large transconductance lets you achieve high single-stage gain. Furthermore, discrete FETs (i.e., those that are not part of an integrated circuit) tend to have higher interelectrode capacitance than BJTs, leading to greater Miller effect (Section 2.19) in common-source amplifiers; the source follower configuration, like the emitter follower, has no Miller effect.

FET followers, with their high input impedance, are commonly used as input stages in oscilloscopes as well as other measuring instruments. There are many applications in which the signal source impedance is intrinsically high, e.g., capacitor microphones, pH probes, charged-particle detectors, or microelectrode signals in biology and medicine. In these cases a FET input stage (whether discrete or part of an integrated circuit) is a good solution. Within circuits there are situations where the following stage must draw little or no current. Common examples are analog "sample-and-hold" and "peak detector" circuits, in which the level is stored on a capacitor and will "droop" if the next amplifier draws significant input current. In all these applications the negligible input current of a FET is more important than its low transconductance, making source followers (or even common-source amplifiers) attractive alternatives to the bipolar emitter follower.

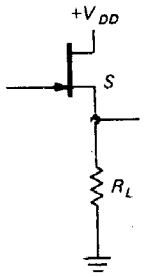


Figure 3.25

Figure 3.25 shows the simplest source follower. We can figure out the output amplitude, as we did for the emitter follower in Section 2.11, using the transconductance. We have

$$v_s = R_L i_d$$

since i_g is negligible; but

$$i_d = g_m v_{gs} = g_m(v_g - v_s)$$

so

$$v_s = \left[\frac{R_L g_m}{(1 + R_L g_m)}\right] v_g$$

For $R_L \gg 1/g_m$ it is a good follower ($v_s \approx v_g$), with gain approaching, but always less than, unity.

Output impedance

The preceding equation for v_s is precisely what you would predict if the source follower's output impedance were equal to $1/g_m$ (try the calculation, assuming a source voltage of v_g in series with $1/g_m$ driving a load of R_L). This is exactly analogous to the emitter follower situation, where the output impedance was $r_e = 25/I_C$, or $1/g_m$. It can be easily shown explicitly that a source follower has output impedance $1/g_m$ by figuring the source current for a signal applied to the output with grounded gate (Fig. 3.26). The drain current is

$$i_d = g_m v_{gs} = g_m v$$

so

$$r_{\text{out}} = v/i_d = 1/g_m$$

typically a few hundred ohms at currents of a few milliamps. As you can see, FET source followers aren't nearly as stiff as emitter followers.

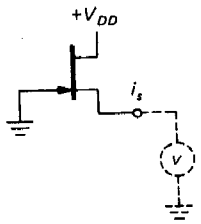


Figure 3.26

There are two drawbacks to this circuit:
1. The relatively high output impedance means that the output swing may be significantly less than the input swing, even with high load impedance, because R_L alone forms a divider with the source's output impedance. Furthermore, because the drain current is changing over the signal waveform, g_m and therefore the output impedance will vary, producing some nonlinearity (distortion) at the output. The situation is improved if FETs of high transconductance are used, of course, but a combination FET–bipolar follower is often a better solution.
2. Because the V_{GS} needed to produce a certain operating current is a poorly controlled parameter in FET manufacture, a source follower has an unpredictable dc offset, a serious drawback for dc-coupled circuits.

Active load

The addition of a few components improves the source follower enormously. Let's take it in stages:

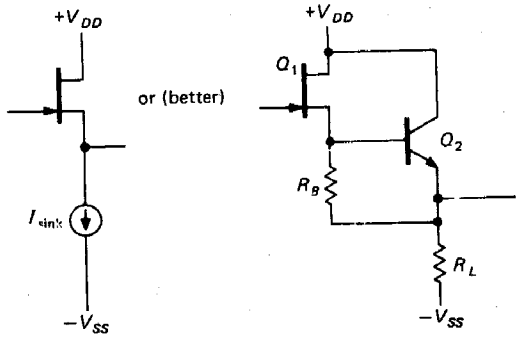


Figure 3.27

First, replace R_L with a (pull-down) current source (Fig. 3.27). The constant source current makes V_{GS} approximately constant, thus reducing nonlinearities. You can think of this as the previous case with infinite R_L, which is what a current source is. The circuit on the right has the advantage of providing low output current, while still providing a (roughly) constant source current of V_{BE}/R_B. We still have the problem of unpredictable (and therefore nonzero) offset voltage (from input to output) of V_{GS} ($V_{GS} + V_{BE}$ for

the circuit on the right). Of course, we could simply adjust I_{sink} to the particular value of I_{DSS} for the given FET (in the first circuit) or adjust R_B (in the second). This is a poor solution, for two reasons: (a) It requires individual adjustment for each FET. (b) Even so, I_D may vary by a factor of two over the normal operating temperature range for a given V_{GS}.

A better circuit uses a matched FET pair to achieve zero offset (Fig. 3.28). Q_1 and Q_2 are a matched pair, on a single chip of silicon. Q_2 sinks a current exactly appropriate to the condition $V_{GS} = 0$. So, for both FETs, $V_{GS} = 0$, and Q_1 is therefore a follower with zero offset. Because Q_2 tracks Q_1 in temperature, the offset remains near zero independent of temperature.

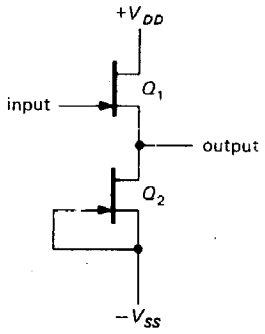


Figure 3.28

You usually see the preceding circuit with source resistors added (Fig. 3.29). A little thought should convince you that R_1 is necessary and that $R_1 = R_2$ guarantees that $V_{out} = V_{in}$ if Q_1 and Q_2 are matched. This circuit modification gives better I_D predictability, allows you to set the drain current to some value less than I_{DSS}, and gives improved linearity, since FETs are better current sources when operated below I_{DSS}. This follower circuit is popular as the input stage for oscilloscope vertical amplifiers.

For the utmost in performance you can add circuitry to bootstrap the drain (eliminating input capacitance) and use a bipolar output stage for low output impedance. That same output signal can then be used to drive an inner "guard" shield in order to effectively eliminate the effects of shielded-cable capacitance, which would otherwise be devastating for the high source impedances that you might see with this sort of high-impedance input buffer amplifier.

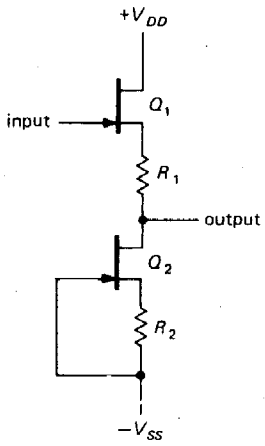


Figure 3.29

3.09 FET gate current

We said at the outset that FETs in general, and MOSFETs in particular, have essentially zero gate current. This is perhaps the most important property of FETs, and it was exploited in the high-impedance amplifiers and followers in the previous sections. It will prove essential, too, in applications to follow – most notably analog switches and digital logic.

Of course, at *some* level of scrutiny we might expect to see some gate current. It's important to know about gate current, because a naive zero-current model is guaranteed to get you in trouble sooner or later. In fact, finite gate current arises from

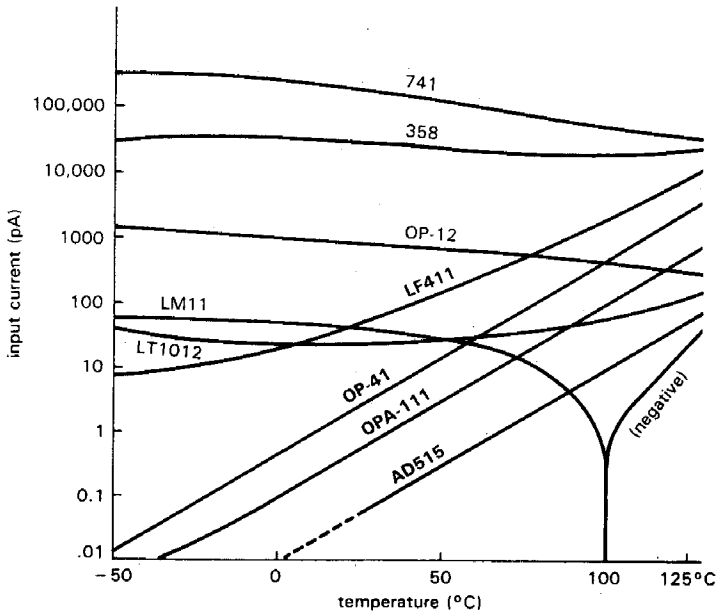


Figure 3.30. The input current of a FET amplifier is gate leakage, which doubles every 10°C.

several mechanisms: Even in MOSFETs the silicon dioxide gate insulation is not perfect, leading to leakage currents in the picoampere range. In JFETs the gate "insulation" is really a back-biased diode junction, with the same impurity and junction leakage current mechanisms as ordinary diodes. Furthermore, JFETs (*n*-channel in particular) suffer from an additional effect known as "impact-ionization" gate current, which can reach astounding levels. Finally, both JFETs and MOSFETs have *dynamic* gate current, caused by ac signals driving the gate capacitance; this can cause Miller effect, just as with bipolar transistors.

In most cases gate input currents are negligible in comparison with BJT base currents. However, there are situations in which a FET may actually have *higher* input current! Let's look at the numbers.

Gate leakage

The low-frequency input impedance of a FET amplifier (or follower) is limited by gate leakage. JFET data sheets usually specify a breakdown voltage, BV_{GSS}, defined as the voltage from gate to channel (source and drain connected together) at which the gate current reaches 1 μA. For smaller applied gate-channel voltages, the gate leakage current, I_{GSS}, again measured with the source and drain connected together, is considerably smaller, dropping quickly to the picoampere range for gate-drain voltages well below breakdown. With MOSFETs you must never allow the gate insulation to break down; instead, gate leakage is specified as some maximum leakage current at a specified gate-channel voltage. Integrated circuit amplifiers with FETs (e.g., FET op-amps) use the misleading term "input bias current," I_B, to specify input leakage current; it's usually in the picoampere range.

The good news is that these leakage currents are in the picoampere range at room temperature. The bad news is that they increase rapidly (in fact, exponentially) with temperature, roughly doubling every 10°C. By contrast, BJT base currents aren't leakage, and in fact tend to *decrease* slightly with increasing temperature. The comparison is shown graphically in Figure 3.30, a plot of input current versus temperature for several IC amplifiers (op-amps).

The FET-input op-amps have the lowest input currents at room temperature (and below), but their input current rises rapidly with temperature, crossing over the curves for amplifiers with carefully designed BJT input stages like the LM11 and LT1012. These BJT op-amps, along with "premium" low-input-current JFET op-amps like the OPA111 and AD549, are fairly expensive. However, we also included everyday "jellybean" op-amps like the bipolar 358 and JFET LF411 in the figure to give an idea of input currents you can expect with inexpensive (less than a dollar) op-amps.

□ JFET impact-ionization current

In addition to conventional gate leakage effects, n-channel JFETs suffer from rather large gate leakage currents when operated with substantial V_{DS} and I_D (the gate leakage specified on data sheets is measured under the unrealistic conditions $V_{DS} = I_D = 0$!). Figure 3.31 shows what happens. The gate leakage current remains near the I_{GSS} value until you reach a critical drain-gate voltage, at which point it rises precipitously. This extra "impact-ionization" current is proportional to drain current, and it rises exponentially with voltage and temperature. The onset of this current occurs at drain-gate voltages of about 25% of BV_{GSS}, and it can reach gate currents of a microamp or more. Obviously a "high-impedance buffer" with a microamp of input current is worthless. That's what you would get if you used a 2N4868A as a follower, running 1mA of drain current from a 40 volt supply.

This extra gate leakage current afflicts primarily n-channel JFETs, and it occurs at higher values of drain-gate voltage. Some cures are to (a) operate at low drain-gate voltage, either with a low-voltage drain supply or with a cascode, (b) use a p-channel JFET, where the effect is much smaller, or (c) use a MOSFET. The most important thing is to be aware of the effect so that it doesn't catch you by surprise.

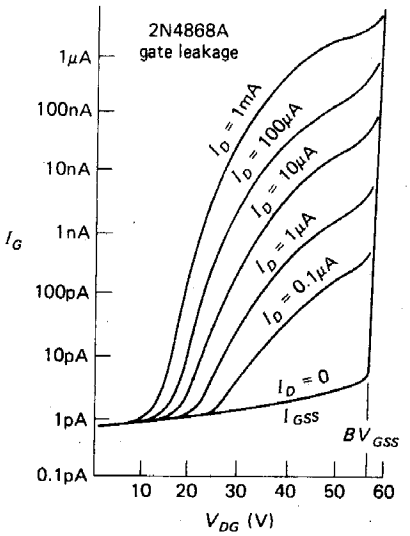


Figure 3.31. JFET gate leakage increases disastrously at higher drain-gate voltages and is proportional to drain current.

□ Dynamic gate current

Gate leakage is a dc effect. Whatever is driving the gate must also supply an *ac* current, because of gate capacitance. Consider a common-source amplifier. Just as with bipolar transistors, you can have the simple effect of input capacitance to ground (called C_{iss}), and you can have the capacitance-multiplying Miller effect (which acts on the feedback capacitance C_{rss}). There are two reasons why capacitive effects are more serious in FETs than in bipolar transistors: First, you use FETs (rather than BJTs) because you want very low input current; thus the capacitive currents loom relatively larger for the same capacitance. Second, FETs often have considerably larger capacitance than equivalent bipolar transistors.

To appreciate the effect of capacitance, consider a FET amplifier intended for a signal source of 100k source impedance.

At dc there's no problem, because the picoampere currents produce only microvolt drops across the signal source's internal impedance. But at 1MHz, say, an input capacitance of 5pF presents a shunt impedance of about 30k, seriously attenuating the signal. In fact, *any* amplifier is in trouble with a high-impedance signal at high frequencies, and the usual solution is to operate at low impedance (50Ω is typical) or use tuned LC circuits to resonate away the parasitic capacitance. The point to understand is that the FET amplifier doesn't look like a 10^{12} ohm load at signal frequencies.

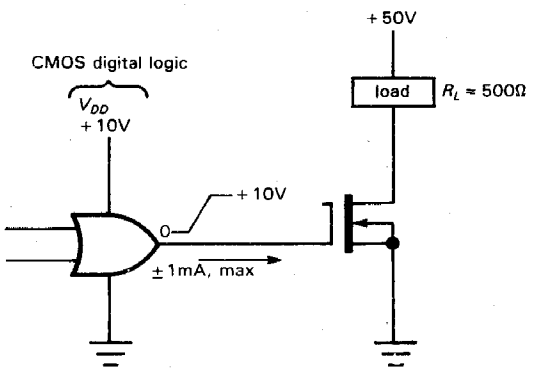


Figure 3.32

As another example, imagine switching a 10 amp load with a power MOSFET (there aren't any power JFETs), in the style of Figure 3.32. One might naively assume that the gate could be driven from a digital logic output with low current-sourcing capability, for example the so-called CMOS logic, which can supply output current on the order of 1mA with a swing from ground to +10 volts. In fact, such a circuit would be a disaster, since with 1mA of gate drive the 350pF feedback capacitance of the 2N6763 would stretch the output switching speed to a leisurely 20μs. Even worse, the dynamic gate currents ($I_{\text{gate}} = CdV_D/dt$) would force currents back into the logic device's output, possibly destroying it via a perverse effect known as "SCR latchup" (more of which in Chapters 8 and 9). Bipolar power transistors turn out to have comparable capacitances, and therefore comparable dynamic input currents; but when you design a circuit to drive a 10-amp power BJT, you're *expecting* to provide 500mA or so of base drive (via a Darlington or whatever), whereas with a FET you tend to take low input current for granted. In this example, once again, the ultra-high-impedance FET has lost some of its luster.

EXERCISE 3.4

Show that the circuit of Figure 3.32 switches in about 20μs, assuming 1mA of available gate drive.