Physics 120 Lab 6 (2019) - Field Effect Transistors: Ohmic Region

The field effect transistor (FET) is a three-terminal device can be used in two extreme ways as an active element in a circuit. One is as a voltage controlled resistance, in the so called "Ohmic" region, for which $V_{DS} < V_{GS} - V_{GS}(off)$. The second is in the so called "Active" region, for which the FET acts as a voltage controlled *current source*.

In the first three exercises, you will use junction FETs (JFETs) to build circuits intended to operate always within the Ohmic region, for which $I_D \propto V_{DS}$. The key is to insure that V_{DS} never gets large enough to push the FET into the Active region.

6-1. Uncompensated attenuator circuit

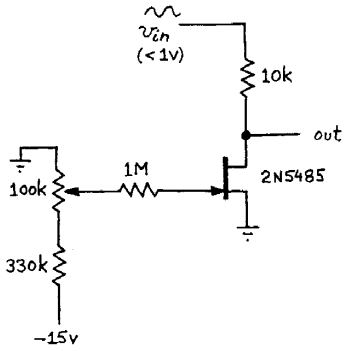

Figure 6.1: N-channel JFET as voltage-controlled resistor: attenuator circuit.

Drive the n-channel JFET circuit in Figure 6.1, using a 2N5485 or 2N5486 JFET, with a small sine wave, with amplitude around 0.2 V and a frequency around 1 kHz. Adjust the potentiometer, using a DMM as a Voltmeter to measure the voltage at the gate, and record the results in terms of variable attenuation of the sine wave; illustrate with **SCREENSHOT**s for at least three different values of V_{GS} (**3 pts**). Comment on the distortion, *e.g.*, harmonic generation, as a function of V_{DS} and illustrate with a **SCREENSHOT** (**2 pt**).

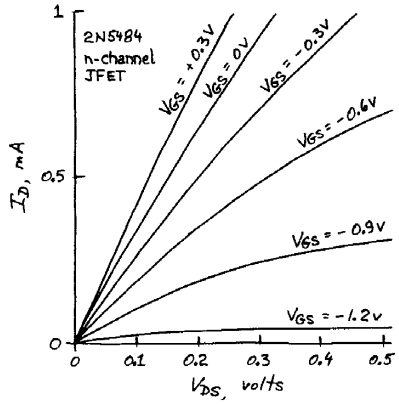

Figure 6.2: FET current source.

6-2 Compensated attenuator circuit

Adding ½ V_{DS} to the gate of the circuit in Figure 6.1 will "linearize" the I_{DS}-V_{DS} curves a good deal, as shown in Figure 6.3; see class notes on this amendment to the circuit. Document, with a **SCREENSHOT**, the effect on the shape of V_{out} as you again drive the circuit with a triangle waveform of ~ 0.2 Volt amplitude and ~ 1 kHz in frequency for at least two different values of $V_{control}$ (**2 pts**).

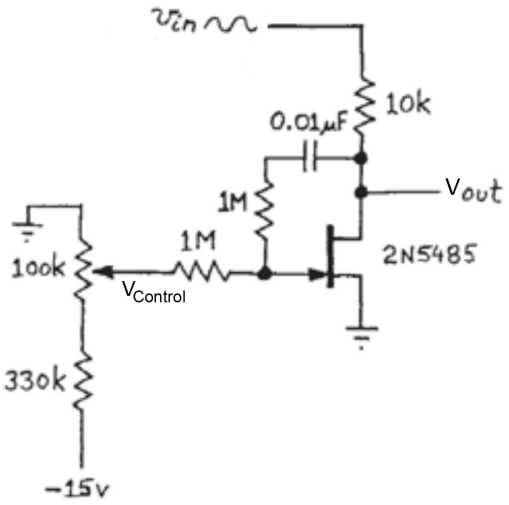

Figure 6.3: Compensated FET as a voltage controlled resistor

6.3 Modulation

We now consider modulation of a high frequency sine (carrier wave) by a low frequency sine (modulation wave). Mind the polarity of the 1 μF electrolytic capacitor as you assemble this circuit (Figure 6.4).

Use the second function generator to add an "AC" component to the "DC" gate potential that you varied with the potentiometer in the circuit of exercise 6.2. The "AC" signal will modulate the attenuation provided by the FET. Choose the frequency of modulation be much lower than the signal, or carrier frequency. Solely a means to start with a working device, try $f_{modulation}$ ~ 40 Hz (or less) with a small amplitude, *i.e.*, $V_{p\text{-}p}$ ~ 0.5 V, $f_{carrier}$ ~ 400 - 4000 Hz with an amplitude of $V_{p\text{-}p}$ ~ 1 - 2 V, and $V_{control}$ ~ -3 V. *Hint: For a stable display, trigger the oscilloscope on the modulating signal and not on the composite output.*

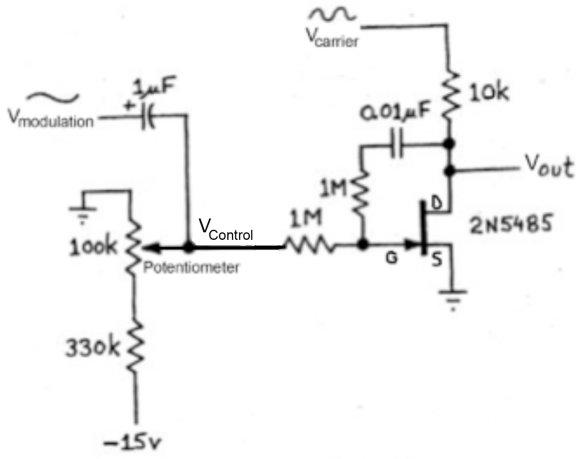

Figure 6.4: Amplitude-modulation of a carrier signal, or multiplication of one signal by another, using a voltage controlled resistor with "DC" and "AC" Control voltages.

Go wild(!) with different modulation amplitudes, frequencies, and but for the record document the output(s) with **SCREENSHOT**s for three different conditions (**6 pts**). Show an output that is a sine wave modulated by a slowly varying sinusoidal envelope as well as, for example, distortion products at sum and difference frequencies. Roughly, at what carrier and modulation frequencies does the circuit begin to fail to function properly, and why (**2 pts**)?

Keep this circuit intact for use with Laboratory Exercise 9.2

6-4 Power MOSFETs

We now switch (no pun intended) to the use of MOSFETs to act at "switches". This exercise involves the control of relatively large currents with a "power" enhancement mode n-channel MOSFET (Figure 6.5). We utilize this MOSFET as an integrated analog switch (Figure 6.6).

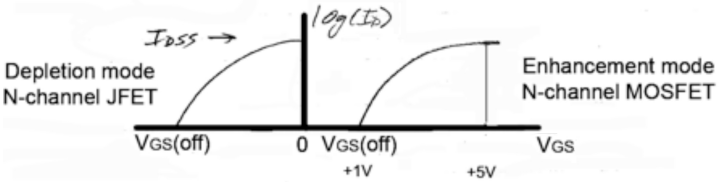

Figure 6.5: I_D versus V_{GS} for the n-channel MOSFET is shifted to positive voltages.

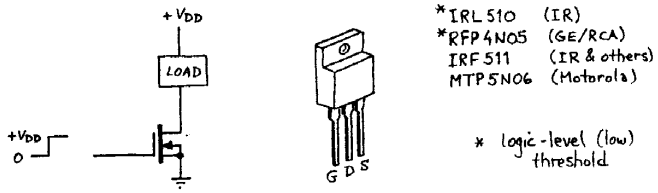

Figure 6.6: Power MOSFET transistor switch.

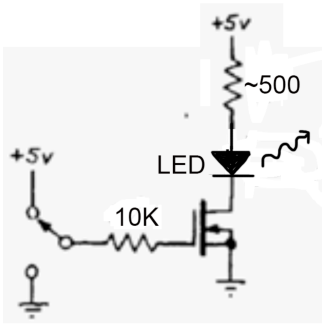

Figure 6.7: MOSFET switching circuit.

Build the circuit shown in Figure 6.7. Use an LED plus current-limiting resistor as the load and confirm that the MOSFET switches when driven through the 10 kΩ resistor at low frequencies; toggle the input between 0 and +5 V by *hand* and illustrate with a **SNAPSHOT** (**2 pts**).

High input impedance is the MOSFET's great strength, so the gate will stay charged if not grounded. Estimate how long the charge will remain (**1 pt**).

6.5. CMOS as solid state switches

CMOS switches are formed by the parallel combination of n-channel and p-channel MOSFETs, so that the combination can conduct both positive and negative going analog signals. Schematically, the CMOS analog switch is extremely simple: it does or does not pass a signal. The next exercises are to familiarize you with these useful and common devices.

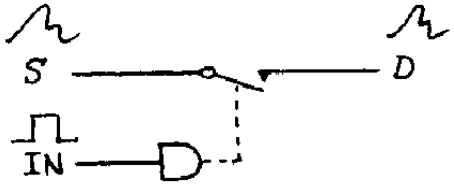

Figure 6.8: Generic picture of an analog switch.

The switch we will use has especially nice properties. It is activated by standard logic voltages, 0 and +5 V (OFF = 0 V and ON = +5 V) (Figure 6.8). It can handle an analog signal anywhere in the range between its positive and negative supply voltages, which we put at ±15 Volts. Lastly, it is a *double-throw* type, which is suited to select between two sources or destinations.

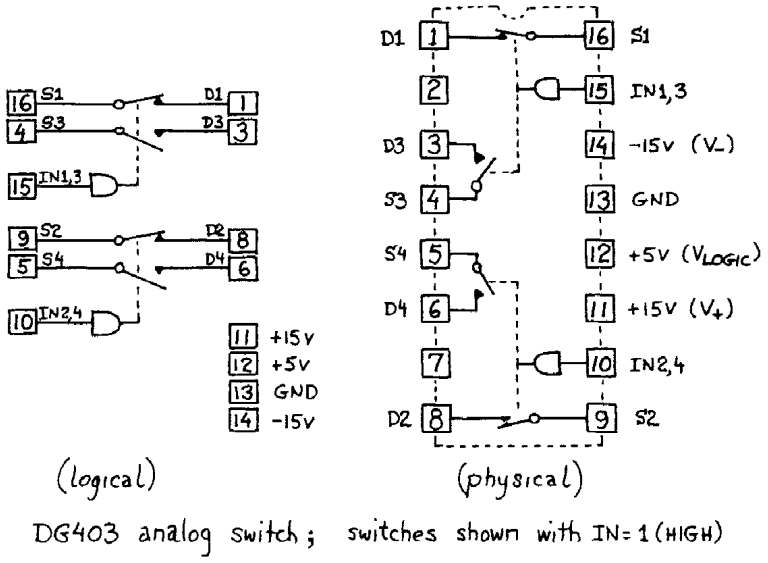

Figure 6.9: DG403 analog switch block diagram and pin out. Each package contains two switches; tie the unused "IN" terminal to ground or to +5 V to ensure that the input to the switch does not hang at a midpoint voltage that can cause excessive heating.

Ideally, the switch should be a short when it is ON. In fact, it shows a small resistance, called R_{ON}. Measure R_{ON}, using the setup shown in Figure 6.10. Use a 1 kHz sine wave at a few Volts as the analog source. Use a wire that you can connect either to ground or to +5 Volts as source of the "digital" signal to turn the CMOS switch ON or OFF. Confirm that the switch does turn ON; document with a **SCREENSHOT** that shows the transition from OFF to ON (**2 pts**). Discuss how you can measure R_{ON}, and do so, making a sketch and showing a **SCREENSHOT** to document your measurement (**2 pts**).

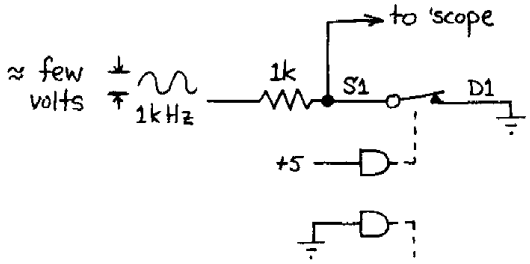

Figure 6.10: R_{ON} measurement.

6.6. Feed-through for CMOS analog switches

The circuit in Figure 6.11 makes the switch perform better: its R_{ON} is negligible relative to the 100 kΩ resistor. Confirm this and document with a **SCREENSHOT** (**1 pt**). When the switch is OFF, does the signal pass through the switch? Try high-frequency sines, start at ~ 10 kHz and scan up to the full 10 MHz of the function generator, and document your results with **SCREENSHOT**s. (**2 pts**). *Note: The small capacitance to ground, C_{in}, in the oscilloscope probe may be more important than the large input resistance, R_{in}, of the probe in distorting the measurement of the output.*

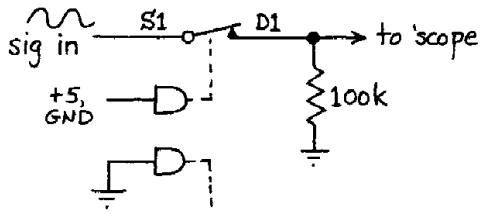

Figure 6.11: More typical application circuit (R_{ON} made negligible).

If signals pass through the OFF switch, why do they pass (**1 pt**)?

6.7. Sample & hold - Example of a CMOS analog switches

This application is used to *sample* a changing waveform, freezing or holding the sampled value while some process occurs, such as conversion from analog into digital form. Build the circuit in Figure 6.12. Demonstrate the "HOLD" and document with a **SCREENSHOT** that includes the transition to holding (**1 pt**).

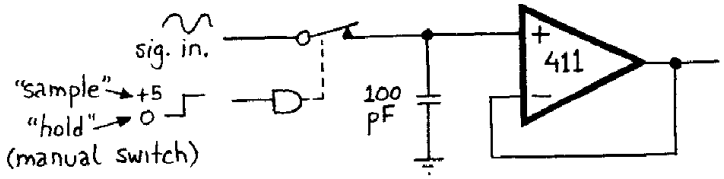

Figure 6.12: Sample and hold

Can you infer from the droop of the signal when the switch is in HOLD position what leakage paths dominate (**2 pts**)? This is not a simple question, in that multiple sources of leakage current may contribute. But give it your best effort, describe your thinking and, if possible, set up a test to confirm or disprove your idea(s).

How does one choose the value of the storage capacitor, 100 pF above (**1 pt**)? What good effects, and what bad effect, would arise from the choice of a capacitor that was either very large or very small (**1 pt**)?

Can you spot the effect of charge injection from the CMOS switch immediately after a transition on the control input? This may be simplest to accomplish with a square wave as the input signal and triggering the oscilloscope off of the op-amp output. Document this with a **SCREENSHOT** (**1 pt**). Compare the voltage effect you would predict, given the specification $Q_{inject} \leq 60$ pC and the value of your storage capacitor, with the observed value (**1 pt**).

32 points total