1. Review of basics
1. $I_G = 0$
2. $I_D = I_S$

In active region, device characteristics are defined by:\[
V_{GS}(off) \leq V_{GS} \leq 0
\]  
4. $V_{DS} > V_{GS} - V_{GS}(off)$; recall that both $V_{GS}$ and $V_{GS}(off)$ are negative

5. $I_D$ is function of $V_{GS}$, with $I_D = \frac{I_{DSS}}{V_{GS}^2(\text{off})} \left[ V_{GS} - V_{GS}(\text{off}) \right]^2$

This implies $I_D = I_{DSS}$ for $V_{GS} = 0$.
6. $I_D$ is independent of $V_{DS}$ (ideal current source)

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1 The turn-off gate-to-source voltage $V_{GS}(off)$ has a number of aliases, such as threshold voltage or pinch-off voltage, denoted $V_{GS}(off) = V_T = V_{TH} = V_P = V_{PO} = V_{P0}$. The active region is also called the "saturation region" or "pentode region", while the Ohmic region is also called the "linear region" or the "triode region". Sigh.
For small changes in gate voltage, we can calculate the changes in source or drain current. The constant of proportionality is referred to as the transconductance, denoted $g_m$, where

$$g_m = \frac{dI_S}{dV_{GS}} = \frac{dI_D}{dV_{GS}} = \frac{2I_{DSS}}{V_{GS}^2\text{(off)}} \left[ V_{GS} - V_{GS\text{(off)}} \right]$$

so that $\Delta I_S = g_m \Delta V_{GS}$. We will see later that the transconductance plays a role analogous to $\beta$ with bipolar junction transistors, but is not a constant, i.e., it depends of $V_{DS}$!
2. Fixed current source

Let's now consider the world's simplest current source.

Here $V_{GS} = 0$, so the current is forced to be $I_{DS} = I_{DSS}$. This is maintained so long as the load line can maintain a value of $V_{DS}$ in the active region, i.e., $V_{DS} > -V_{GS}$(off).

The load line is given by writing Kirchoff's rule for voltage drops and ignoring the transconductance $1/g_m$:

$$0 = -V_{DD} + I_{DS} R_{Load} + V_{DS}$$

to yield the load line $I_{DS} = \frac{V_{DD} - V_{DS}}{R_{Load}}$.

This must intercept $I_{DS} = I_{DSS}$ in the active region. Here, we slide along the (flat) line of $I_D = I_{DSS}$ so long as $V_{DS} > -V_{GS}$(off).

To find the maximum load resistance that keeps us in the active zone, we first rewrite the load line as an expression for $V_{DS}$, i.e.,

$$V_{DS} = V_{DD} - I_{DSS} R_{Load}$$

Noting that $V_{DS} > -V_{GS}$(off), this implies

$$-V_{GS}(off) > V_{DD} - I_{DSS} R_{Load}$$

or

$$R_{Load} < \frac{V_{DD} + V_{GS}(off)}{I_{DSS}}$$

This simple device suffers only from having a value of $I_D$ that is not adjustable! Yet for example, the (2N5485), has $I_{DSS} = 8$ mA, enough to drive a typical LED with the effective resistance of $R_L \sim 100 \ \Omega$. 
3. Improved current source

A more sophisticated source uses a resistor between the source and ground to determine $I_{DS}$.

Here we have $V_G = 0$ but $V_{GS} < 0$, since the gate is grounded. The loop equation encompassing the gate and source satisfies (ignoring the transconductance term $1/g_m$):

$$0 = -V_G + V_{GS} + I_{DS} R_S$$

or, with $V_G = 0$, $I_{DS} = -\frac{V_{GS}}{R_S}$.

We need to choose a value of $R_S$ to fix $I_D$. The second equation that relates $I_{DS}$ and $V_{GS}$ is the constitutive equation

$$I_{DS} = \frac{I_{DSS}}{V_{GS}^2} \left[ V_{GS} - V_{GS}^{(off)} \right]^2 = I_{DSS} \left( 1 - \frac{V_{GS}}{V_{GS}^{(off)}} \right)^2$$

We are free to pick a desired quiescent current, denoted $I_{DSQ}$, with $I_{DSQ} < I_{DSS}$. Then the required value of $R_S$ is found by substituting $V_{GS} = -I_{DSQ} R_S$ into the constitutive equation, i.e.,

$$I_{DSQ} = I_{DSS} \left( 1 + \frac{I_{DSQ} R_S}{V_{GS}^{(off)}} \right)^2$$

Thus $R_S = -\frac{V_{GS}^{(off)}}{I_{DSQ}} \left( 1 - \sqrt{\frac{I_{DSQ}}{I_{DSS}}} \right)$.

The load line is given by writing Kirchoff's rule for voltage drops in the outer loop and ignoring the transconductance $1/g_m$:
0 = -V_{DD} + I_{DSQ} R_{Load} + V_{DS} + I_{DSQ} R_S.

We first consider the bounds of $R_{Load}$. The load-line is rearranged to

$V_{DS} = V_{DD} - I_{DSQ} R_{Load} - I_{DSQ} R_S.$

The requirement that $V_{DS} > V_{GS} - V_{GS}(\text{off})$ in the active region leads to

$V_{GS} - V_{GS}(\text{off}) < V_{DD} - I_{DSQ} R_{Load} - I_{DSQ} R_S.$

But $V_{GS} = -I_{DSQ} R_S$ from our analysis of the inner loop. Thus

$-V_{GS}(\text{off}) < V_{DD} - I_{DSQ} R_{Load}$ or

$R_{Load} < \frac{V_{DD} + V_{GS}(\text{off})}{I_{DSQ}}.$

We return to the load line equation, which is reordered as

The load line for $I_D$ versus $V_{DS}$ is found by computing the voltage drops along the loop, i.e.,

$I_{DS} = \frac{V_{DD} - V_{DS}}{R_{Load} + R_S}.$

The value of $V_{DSQ}$ varies for $I_{DSQ}$ fixed as $R_{Load}$ varies.

The FET current sources are independent of fluctuations in the power supply voltage and largely independent of $g_m$.

As an example relevant to the laboratory exercise with a 2N5485, the choice $I_{DSQ} = 0.4$ mA with $I_{DSS} = 8$ mA and $V_{GS}(\text{off}) = -3$ V, we find $R_S = 5.8$ kΩ. We use the closest value 5% resistor at 5.6 kΩ.

4. Source follower

The analysis is over two loops, one to define $R_s$ and the other to define the load line.
We consider the bottom loop to relate $V_{in}$ and $I_D$:
\[ 0 = -V_{in} + V_{GS} + R_S I_S \]
so
\[ I_D = \frac{V_{in} - V_{GS}}{R_S}. \]

We consider the top loop to relate $V_{out}$ and $I_D$:
\[ 0 = -V_{DD} + V_{DS} + R_S I_D \]
so
\[ I_D = \frac{V_{DD} - V_{DS}}{R_S} = \frac{V_{out}}{R_S} \]
and we get
\[ V_{out} = I_D R_S = V_{in} - V_{GS}. \]
We see that the output follows the input with the addition of a term $V_{GS}$. Recall that $V_{GS} < 0$ so the offset is positive.

The value of $V_{GS}$ is found from the intersection of the load line
\[ I_D = \frac{V_{in} - V_{GS}}{R_S} \]
and the constitutive equation
\[ I_D = I_{bss} \left[ \frac{V_{GS} - V_{GS}(\text{off})}{V_{GS}(\text{off})^2} \right]^2. \]

The critical issue is that $V_{GS}$ is not constant but depends on $V_{in}$! This leads to a nonlinearity, yet is minimal for the choice $V_{in} \ll V_{GS}(\text{off})$, as seen by solving for $V_{GS}$, i.e.,
\[ V_{GS} = V_{GS}(\text{off}) \left[ 1 - \frac{V_{GS}(\text{off})}{2 R_{bss}} + \sqrt{\left( \frac{V_{GS}(\text{off})}{2 R_{bss}} \right)^2 + \frac{V_{in} - V_{GS}(\text{off})}{R_{bss}}} \right]. \]

We'll next see how to cancel the $V_{GS}$ term, but before then we consider the inclusion of a nonzero value of $1/g_m$ as a resistance from the gate to the source. The loop equation is:
\[ 0 = -V_{in} + V_{GS} + (1/g_m) I_S + R_S I_S \]
so
\[ I_D = \frac{V_{in} - V_{GS}}{R_S + 1/g_m} \]
and
\[ V_{out} = I_D R_S = \frac{g_m R_S}{1 + g_m R_S} (V_{in} - V_{GS}). \]

The key is to maintain $R_s g_m \gg 1$ or $R_s \ll 1/g_m$. This is critical, as $g_m$ is also a function of $V_{GS}$. 
4. Improved voltage follower

An improved follower may be built in which the offset voltage $V_{GS}$ is minimized. We use a current source to define the current through $R_s$, as show below.

Here we may write an expression for the equilibrium current (ignoring $g_m$):

$$0 = -V_{in} + V_{GS}(Q_1) + I_{DQ} R_1 + V_{out}$$

But we previously solved for the self limiting current source corresponding to the lower JFET, or $I_{DQ} = -\frac{V_{GS}(Q_2)}{R_2}$.

Then

$$0 = -V_{in} + V_{GS}(Q_1) - \frac{V_{GS}(Q_2)}{R_2} R_1 + V_{out}$$

For $R_1 = R_2$ and matched JFETs, i.e., $V_{GS}(Q_1) = V_{GS}(Q_2)$, the output voltage is exactly the input voltage and we have a perfect follower with a very large input impedance.

"Matched" means that $I_{DSS}$ and $V_{GS}(\text{off})$ are the same for each of the two FETs, so that $V_{GS}(Q_1) = V_{GS}(Q_2)$ since the same current $I_{DS}$ flows through each FET. In fact, one can purchase FETs that are manufactured as pairs, on a common substrate, for this purpose.