



Ultra-Low Offset Voltage Op Amp

AD OP-07

FEATURES

Ten Times More Gain Than Other OP-07 Devices
(3.0M min)

Ultra-Low Offset Voltage: $10\mu\text{V}$

Ultra-Low Offset Voltage Drift: $0.2\mu\text{V}/^\circ\text{C}$

Ultra-Stable vs. Time: $0.2\mu\text{V}/\text{month}$

Ultra-Low Noise: $0.35\mu\text{V p-p}$

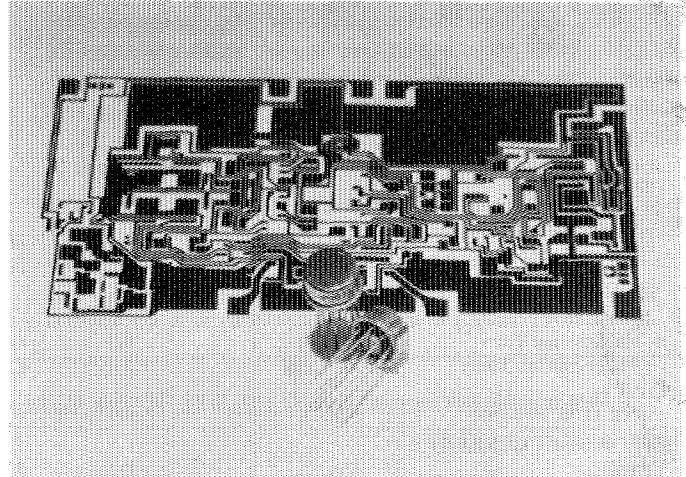
No External Components Required

Monolithic Construction

High Common Mode Input Range: $\pm 14.0\text{V}$

Wide Power Supply Voltage Range: $\pm 3\text{V}$ to $\pm 18\text{V}$

Fits 725, 108A/308A Sockets



PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed loop gain applications. Input offset voltages as low as $10\mu\text{V}$, bias currents of 0.7nA , internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of $0.2\mu\text{V}/^\circ\text{C}$ and long-term stability of $0.2\mu\text{V}/\text{month}$ eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common mode input voltage range ($\pm 14\text{V}$) high common mode rejection ratio (up to 126dB) and high differential input impedance ($50\text{M}\Omega$); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to $+70^\circ\text{C}$ temperature range, while the AD OP-07A and AD OP-07 are specified for -55°C to $+125^\circ\text{C}$ operation. Processing to the requirements of MIL-STD-883, Class B, is available on the AD OP-07 and AD OP-07A. The devices are packaged in either TO-99 hermetically-sealed metal cans or plastic 8-pin mini DIPS.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultra-low offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultra-low input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

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SPECIFICATIONS ($T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified)

| MODEL | PARAMETER | SYMBOL | AD OP-07E | | | AD OP-07C | | | AD OP-07D | | | | |
|-----------------------------|-----------------------------|------------------|-------------------|--------------------|-------------|-------------|------------|-----------|--------------|------------|--------------|--------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| OPEN LOOP GAIN | A_{VO} | | 2,000 | 5,000 | | 1,200 | 4,000 | | 1,200 | 4,000 | | | |
| | | | 1,800 | 4,500 | | 1,000 | 4,000 | | 1,000 | 4,000 | | | |
| | | | 300 | 1,000 | | 300 | 1,000 | | 300 | 1,000 | | | |
| OUTPUT CHARACTERISTICS | Maximum Output Swing | V_{OM} | ± 12.5 | ± 13.0 | | ± 12.0 | ± 13.0 | | ± 12.0 | ± 13.0 | | | |
| | | | ± 12.0 | ± 12.8 | | ± 11.5 | ± 12.8 | | ± 11.5 | ± 12.8 | | | |
| | | | ± 10.5 | ± 12.0 | | | ± 12.0 | | | | | | |
| | | | ± 12.0 | ± 12.6 | | ± 11.0 | ± 12.6 | | ± 11.0 | ± 12.6 | | | |
| Open-Loop Output Resistance | R_O | | 60 | | 60 | | 60 | | 60 | | | | |
| | | | | | | | | | | | | | |
| FREQUENCY RESPONSE | Closed Loop Bandwidth | BW | | 0.6 | | 0.6 | | | 0.6 | | | | |
| | Slew Rate | SR | | 0.17 | | 0.17 | | | 0.17 | | | | |
| INPUT OFFSET VOLTAGE | Initial | V_{OS} | | 30 | 75 | | 60 | 150 | | 60 | 150 | | |
| | | | | 45 | 130 | | 85 | 250 | | 85 | 250 | | |
| | Adjustment Range | | | ± 4 | | | ± 4 | | | ± 4 | | | |
| | | | | | | | | | | | | | |
| | Average Drift | No External Trim | TCV_{OS} | | 0.3 | 1.3 | | 0.5 | 1.8 (Note 3) | | 0.7 | 2.5 (Note 3) | |
| | | | | With External Trim | TCV_{OSN} | | 0.3 | 1.3 | | 0.4 | 1.6 (Note 3) | | 0.7 |
| Long Term Stability | V_{OS}/Time | | 0.3 | 1.5 | | 0.4 | 2.0 | | 0.5 | 3.0 | | | |
| INPUT OFFSET CURRENT | Initial | I_{OS} | | 0.5 | 3.8 | | 0.8 | 6.0 | | 0.8 | 6.0 | | |
| | | | | 0.9 | 5.3 | | 1.6 | 8.0 | | 1.6 | 8.0 | | |
| | | | Average Drift | TCI_{OS} | 8 | 35 (Note 3) | | 12 | 50 (Note 3) | | 12 | 50 (Note 3) | |
| INPUT BIAS CURRENT | Initial | I_B | | ± 1.2 | ± 4.0 | | ± 1.8 | ± 7.0 | | ± 2.0 | ± 12 | | |
| | | | | ± 1.5 | ± 5.5 | | ± 2.2 | ± 9.0 | | ± 3.0 | ± 14 | | |
| | | | Average Drift | TCI_B | 13 | 35 (Note 3) | | 18 | 50 (Note 3) | | 18 | 50 (Note 3) | |
| INPUT RESISTANCE | Differential | R_{IN} | 15 | 50 | | 8 | 33 | | 7 | 31 | | | |
| | Common Mode | $R_{IN\ CM}$ | | 160 | | | 120 | | | 120 | | | |
| INPUT NOISE | Voltage | $e_n\ P-P$ | | 0.35 | 0.6 | | 0.38 | 0.65 | | 0.38 | 0.65 | | |
| | | | Voltage Density | e_n | | 10.3 | 18.0 | | 10.5 | 20.0 | | 10.5 | 20.0 |
| | | | | | | 10.0 | 13.0 | | 10.2 | 13.5 | | 10.2 | 13.5 |
| | Current | $i_n\ P-P$ | | 9.6 | 11.0 | | 9.8 | 11.5 | | 9.8 | 11.5 | | |
| | | | Current Density | i_n | | 14 | 30 | | 15 | 35 | | 15 | 35 |
| | | | | | | 0.32 | 0.80 | | 0.35 | 0.90 | | 0.35 | 0.90 |
| | | | 0.14 | 0.23 | | 0.15 | 0.27 | | 0.15 | 0.27 | | | |
| | | | 0.12 | 0.17 | | 0.13 | 0.18 | | 0.13 | 0.18 | | | |
| INPUT VOLTAGE RANGE | Common Mode | $CMVR$ | ± 13.0 | ± 14.0 | | ± 13.0 | ± 14.0 | | ± 13.0 | ± 14.0 | | | |
| | | | ± 13.0 | ± 13.5 | | ± 13.0 | ± 13.5 | | ± 13.0 | ± 13.5 | | | |
| | Common Mode Rejection Ratio | $CMRR$ | 106 | 123 | | 100 | 120 | | 94 | 110 | | | |
| | | | 103 | 123 | | 97 | 120 | | 94 | 106 | | | |
| POWER SUPPLY | Current, Quiescent | I_Q | | 3.0 | 4.0 | | 3.5 | 5.0 | | 3.5 | 5.0 | | |
| | | | Power Consumption | P_D | | 90 | 120 | | 105 | 150 | | 105 | 150 |
| | Rejection Ratio | $PSRR$ | | 6.0 | 8.4 | | 6.0 | 8.4 | | 6.0 | 8.4 | | |
| | | | | 94 | 107 | | 90 | 104 | | 90 | 104 | | |
| | | | 90 | 104 | | 86 | 100 | | 86 | 100 | | | |
| OPERATING TEMPERATURE RANGE | T_{min}, T_{max} | | 0 | +70 | | 0 | +70 | | 0 | +70 | | | |
| PACKAGE STYLE | "N" Package | | | | | | | | | | | | |
| | 8-Pin Mini DIP | | AD OP-07EN | | AD OP-07CN | | AD OP-07DN | | | | | | |
| | "H" Package | | | | | | | | | | | | |
| | TO-99 | | AD OP-07EH | | AD OP-07CH | | AD OP-07DH | | | | | | |

NOTES:

¹The AD OP-07A and AD OP-07 are available processed to MIL-STD-883, Class B. Order AD OP-07AH-883B or AD OP-07H-883B.

²Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, AD OP-07A offset voltage is measured five minutes after power supply application at 25°C , -55°C and $+125^\circ\text{C}$.

³Parameter is not 100% tested; 90% of units meet this specification.

⁴Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu\text{V}$ – Parameter is not 100% tested; 90% of units meet this specification.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

| | |
|-------------------------------------|------------|
| Supply Voltage | ±22V |
| Internal Power Dissipation (Note 1) | 500mW |
| Differential Input Voltage | ±30V |
| Input Voltage (Note 2) | ±22V |
| Output Short Circuit Duration | Indefinite |

| | |
|---|-----------------|
| Storage Temperature Range | -65°C to +150°C |
| Operating Temperature Range | |
| OP-07A, OP-07 | -55°C to +125°C |
| OP-07E, OP-07C, OP-07D | 0 to +70°C |
| Lead Temperature Range (Soldering, 60sec) | 300°C |

NOTES:

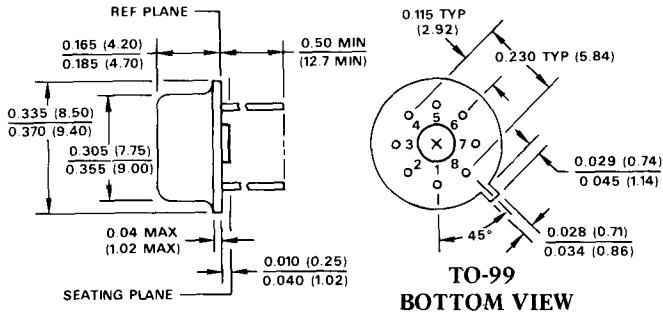
Note 1: Maximum package power dissipation vs. ambient temperature.

| Package Type | Maximum Ambient Temperature for Rating | Derate Above Maximum Ambient Temperature |
|--------------|--|--|
| TO-99 (H) | 80°C | 7.1mW/°C |

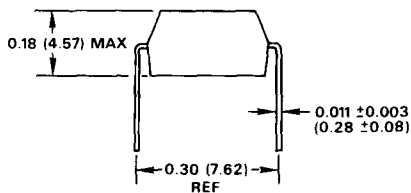
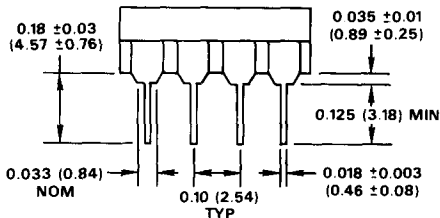
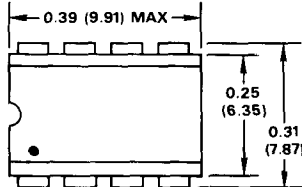
Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

OUTLINE DIMENSIONS

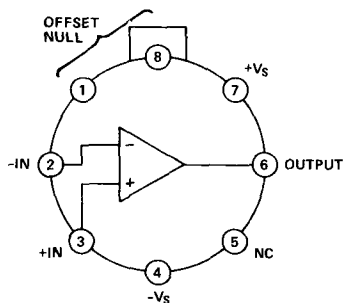
Dimensions shown in inches and (mm).



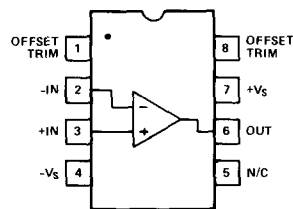
H-PACKAGE



N-PACKAGE PIN CONFIGURATION TOP VIEW



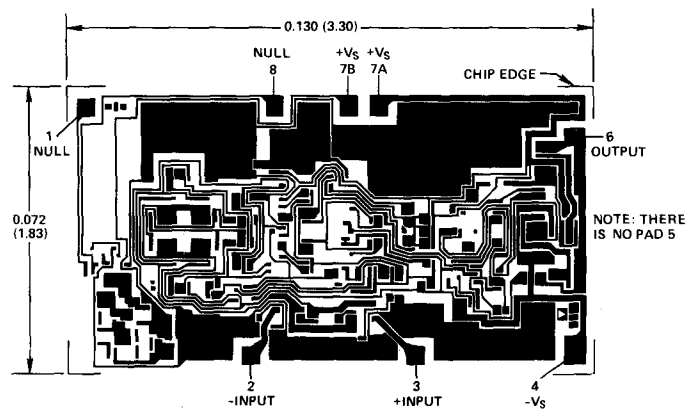
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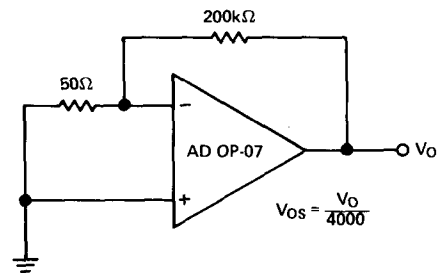
N-PACKAGE

CHIP DIMENSIONS AND BONDING DIAGRAM

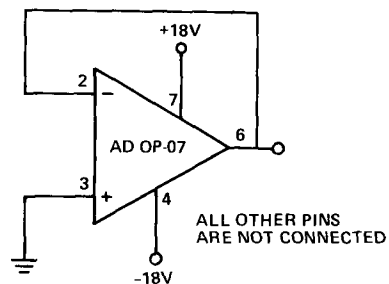
Dimensions shown in inches and (mm).



The AD OP-07 is available in wafer-trimmed chip form for precision hybrids. Consult the factory directly for details.



Offset Voltage Test Circuit



Burn-In Circuit

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be re-

moved (or referenced to $+V_S$). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

The AD OP-07 provides stable operation with load capacitances up to 500pF and $\pm 10V$ swings; larger capacitances should be decoupled with 50 Ω resistor.

Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01 μF ceramic capacitor as shown in Figure 1.

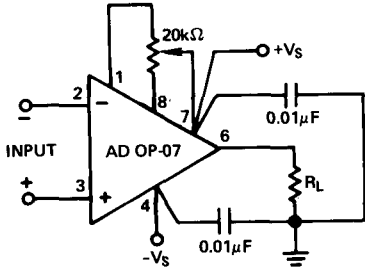
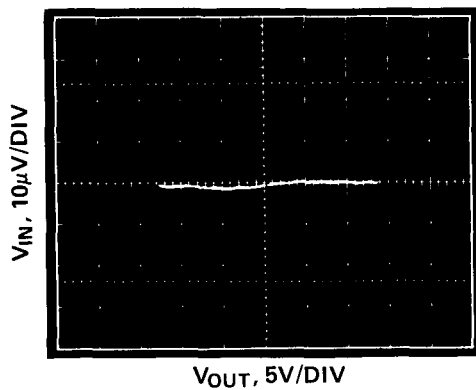
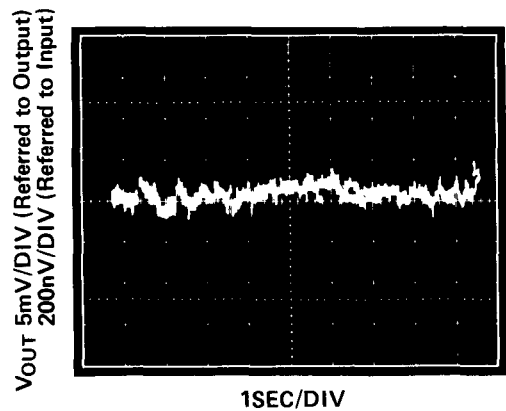


Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

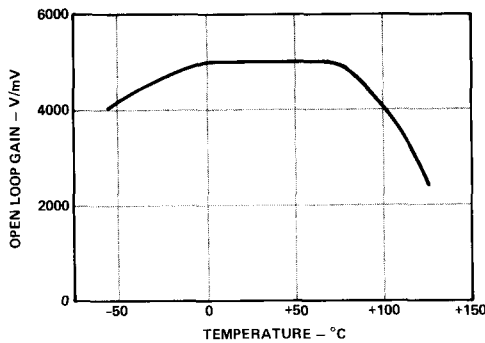
Performance Curves (typical @ $T_A = +25^\circ C$, $V_S = \pm 15V$, AD OP-07 Grade Device unless otherwise noted)



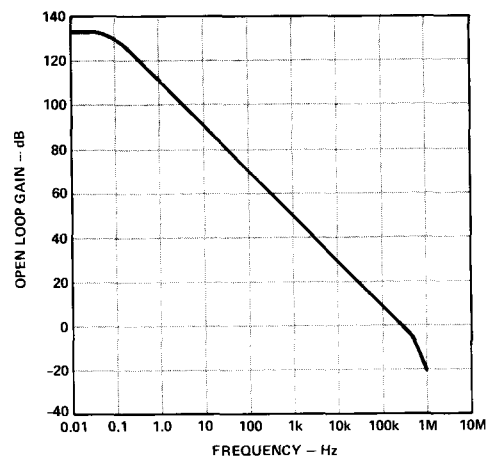
AD OP-07 Open Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

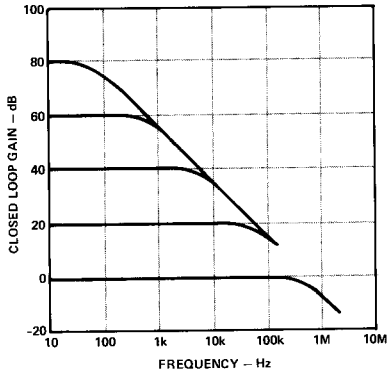


Open Loop Gain vs. Temperature

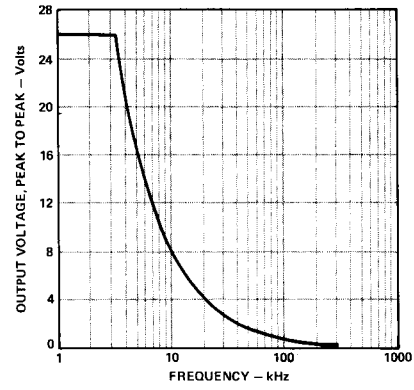


Open Loop Frequency Response

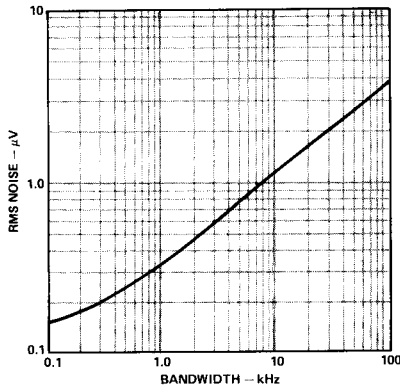
Typical Performance Curves



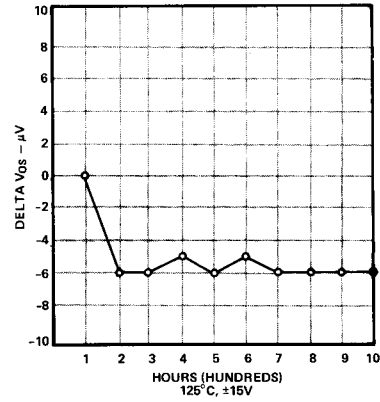
Closed Loop Response for Various Gain Configurations



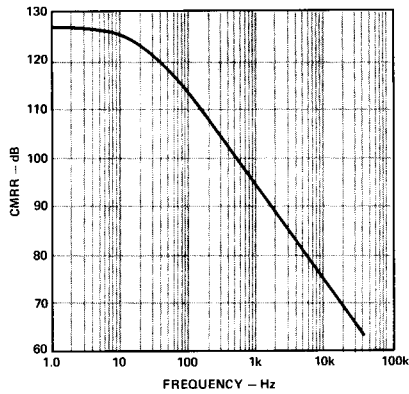
Maximum Undistorted Output vs. Frequency



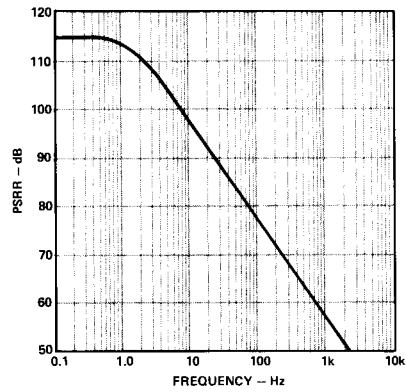
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



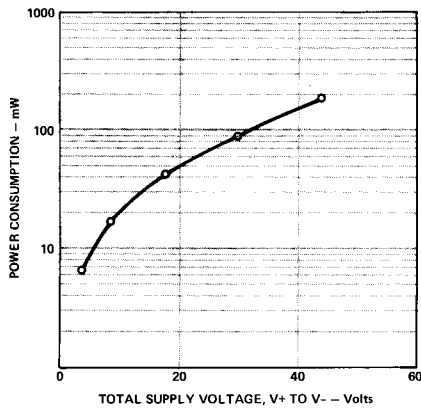
Offset Voltage vs. Time



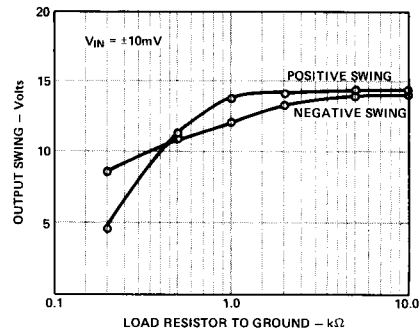
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance