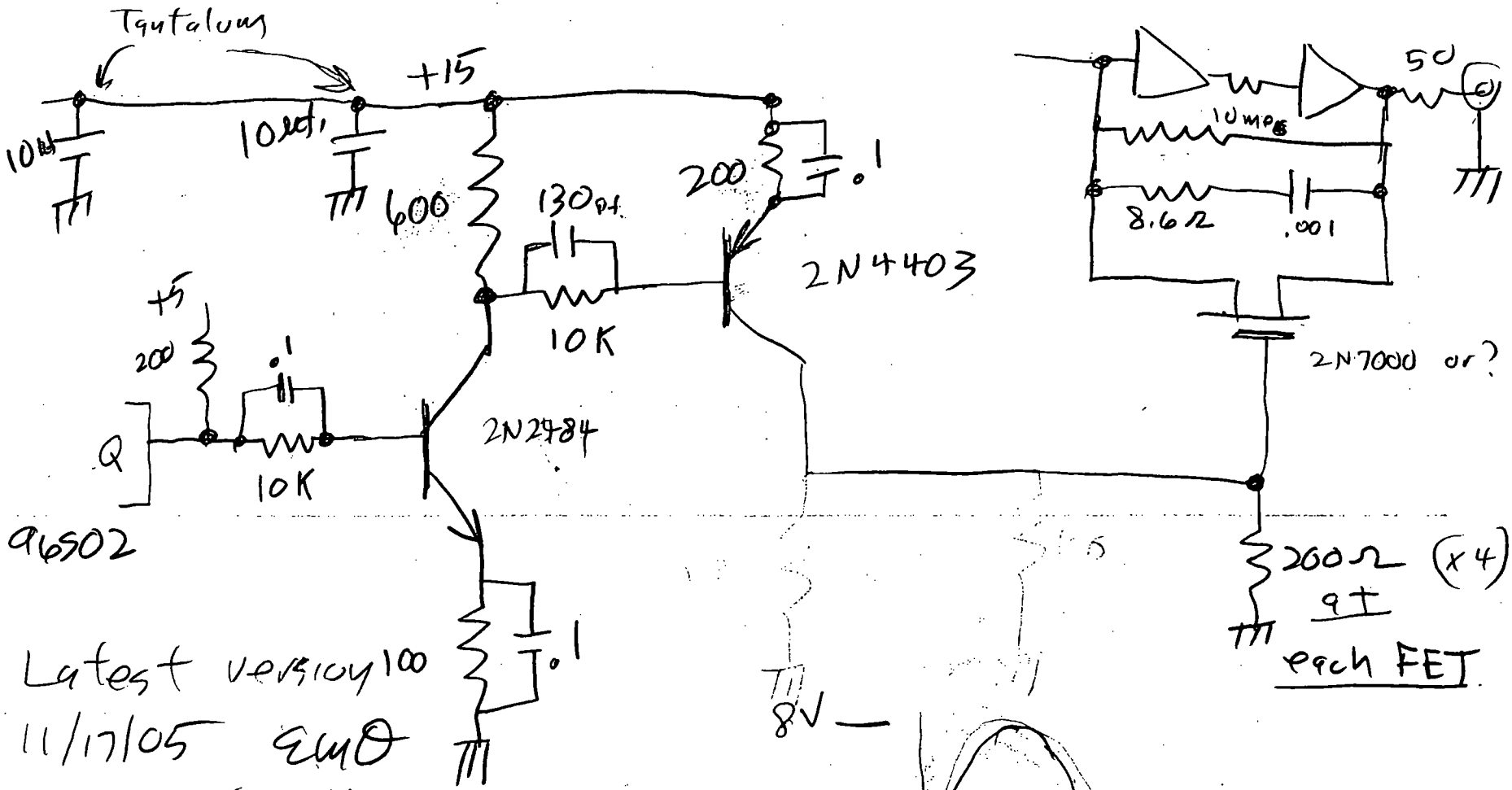
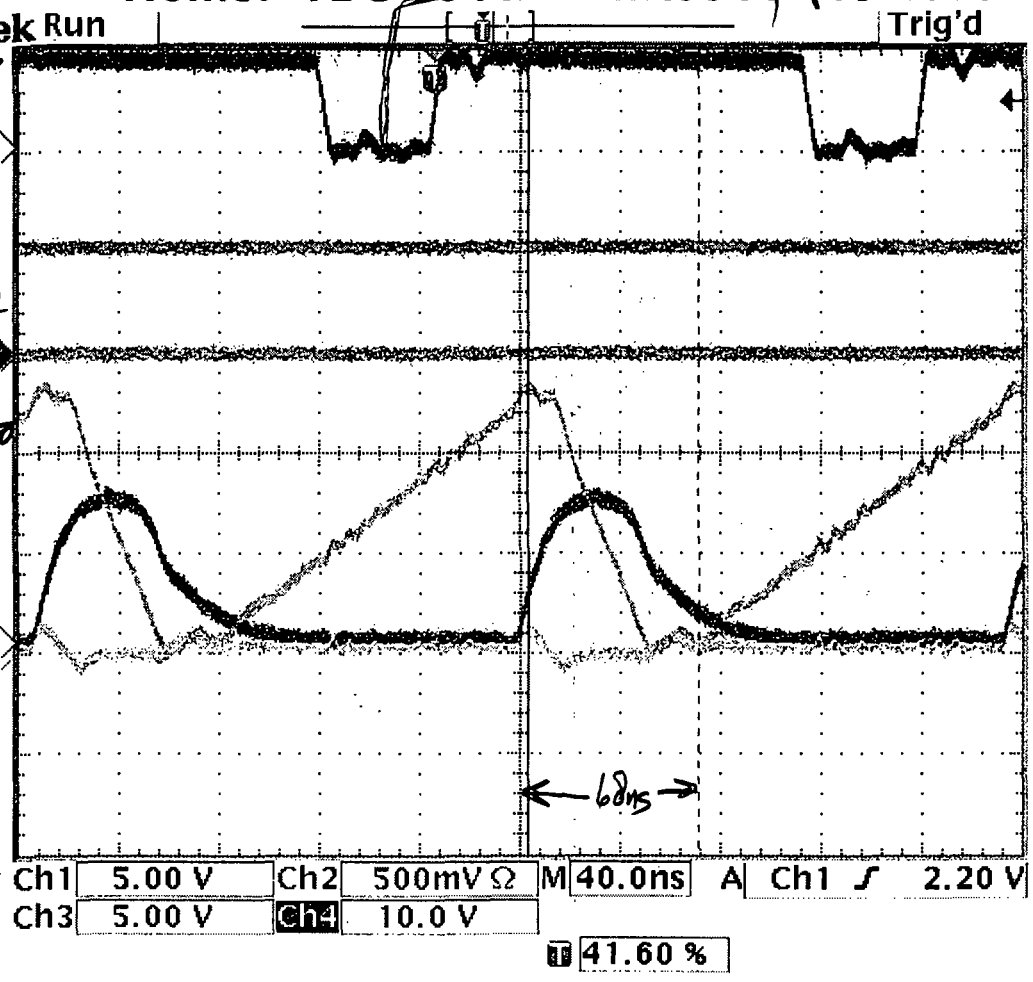


Latest version 100
11/17/05 EMO
See attached
waveforms

Pixel Clock 5.175 MHz

Home: TDS ~~3044B TEK3044~~ (192.168.0.60)



10V Square wave

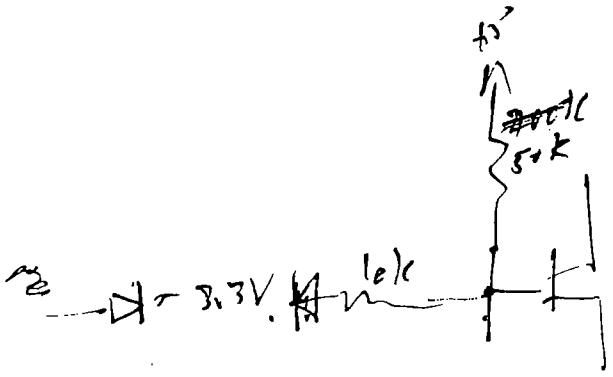
Integrated Ramp

8V

Reset Pulse

Changes: Each FET Gate has 200Ω to ground.

8.6 Ω Resistor in series with each Cap.



$\frac{1.7V}{10k}$

Buffer

Inverter

must be positive

Inverting Integrator/Output Driver

CH1_IN

CH1_BYPASS

CH1 INTEGRATION TIME

PIXEL CLK

Reset

Delay

Integrator Reset

$f_{cut} = 17\,Hz$

50–80 ns

(20→40 ns)

Delay ~10 ns to ~60–100 ns

Reset width 10 ns to 50 ns

PHYSICS ELECTRONICS SHOP

Title: 4 Channel Integrator

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D driver

450 ns → 200 ns

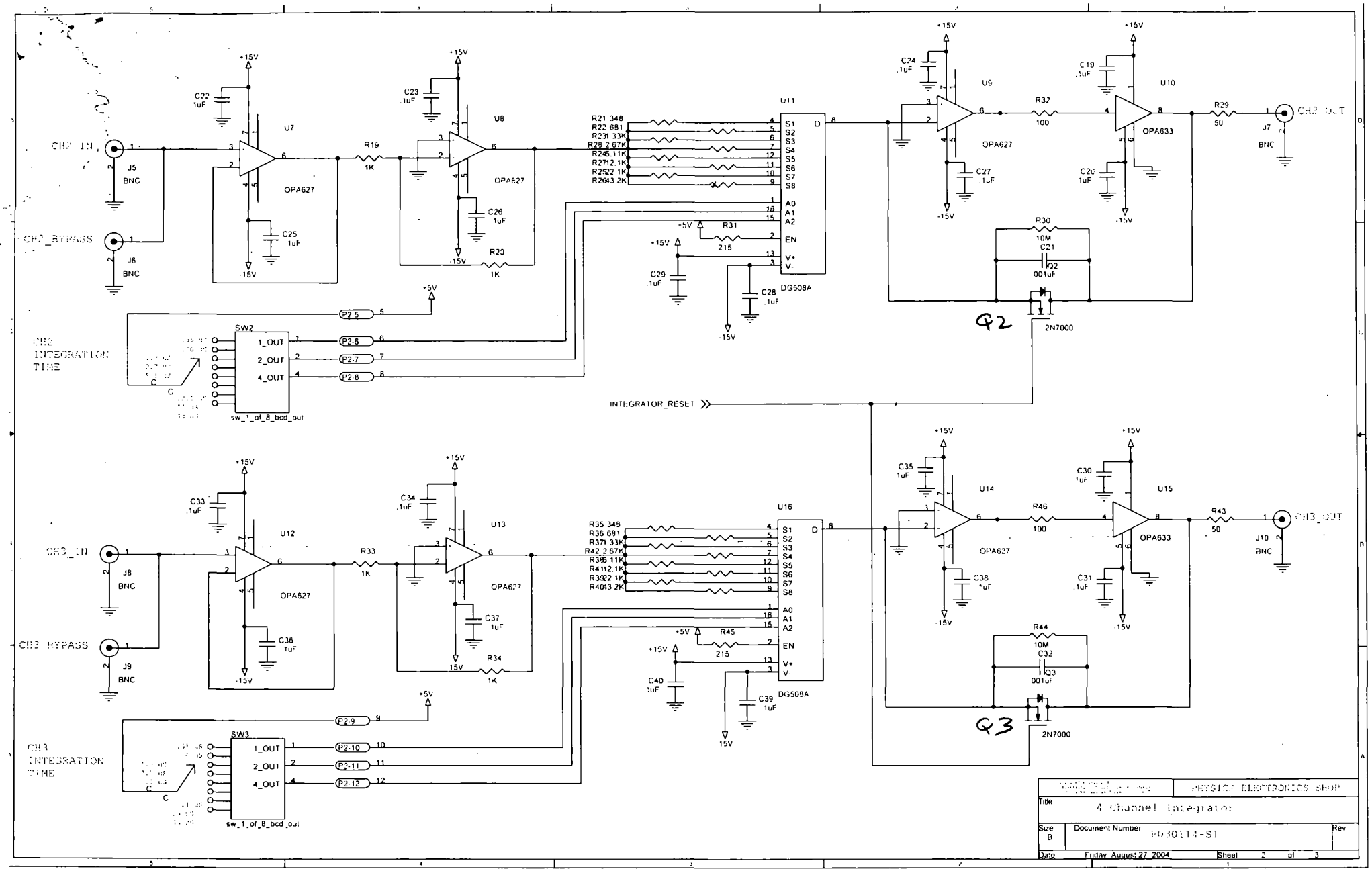
changes: R15, 18, 61, 62 100 Ω

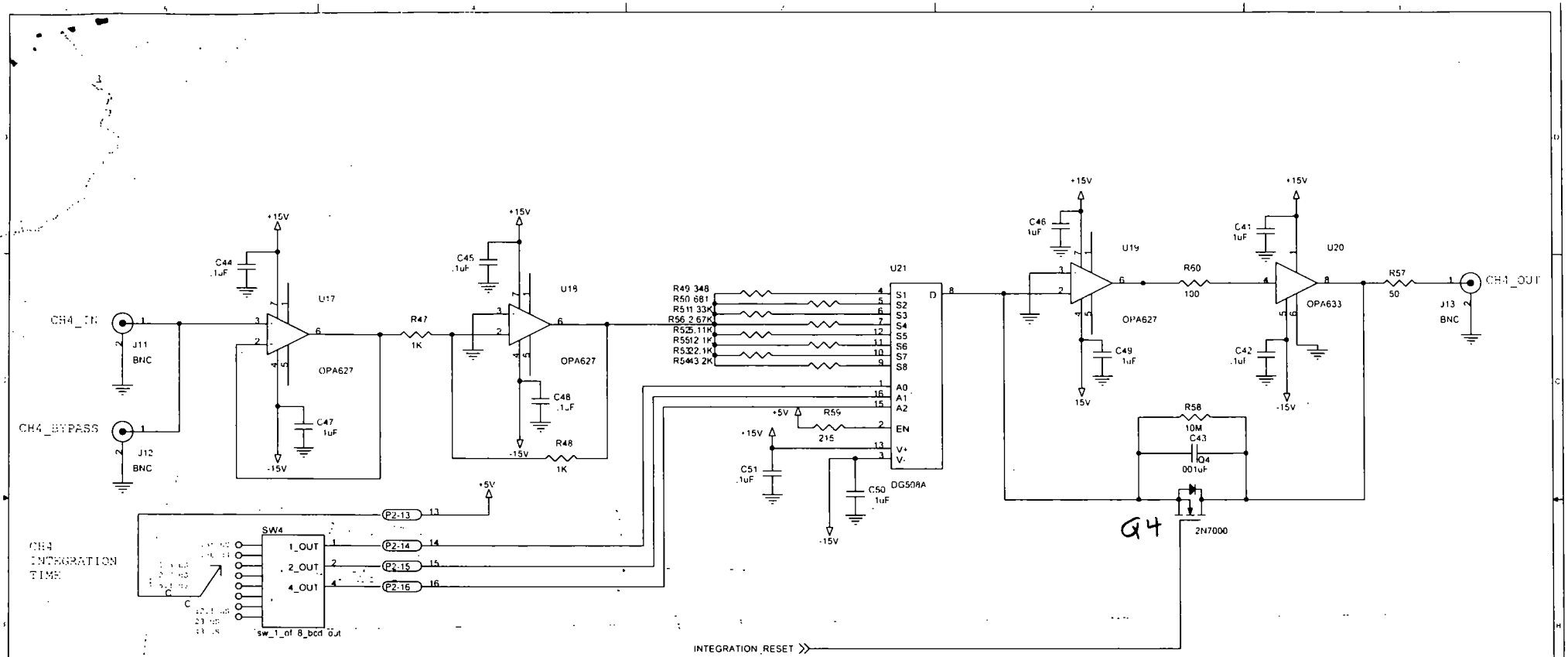
C17, 18 ~~43pF~~ Removed

Q1 ~~2N4401~~ (See Revised Driver)

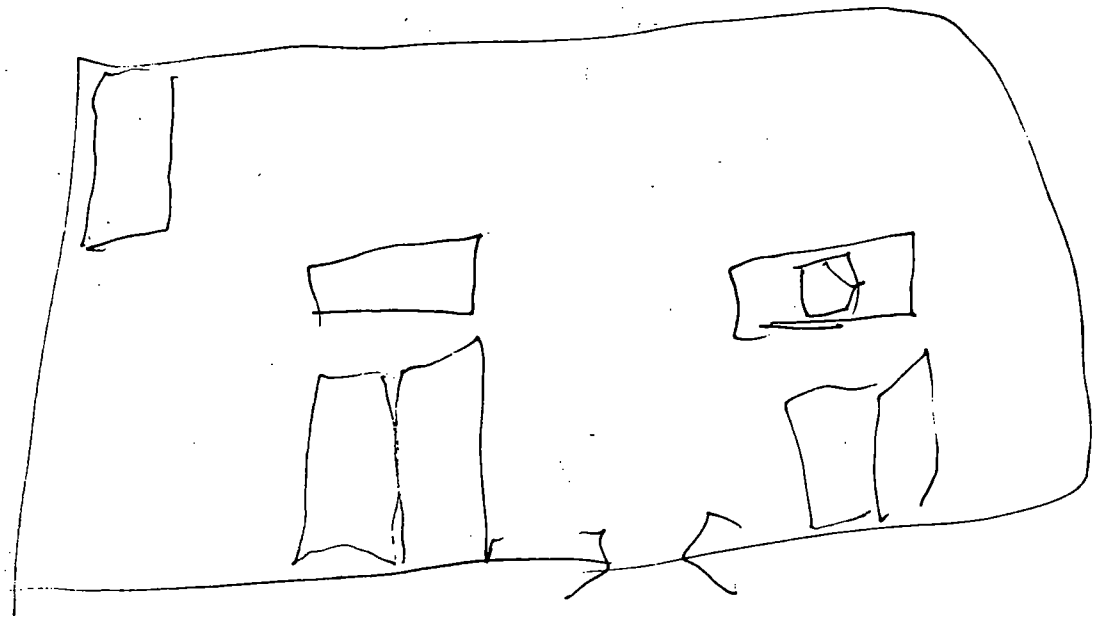
Q2, 3, 4, 5 2N7000

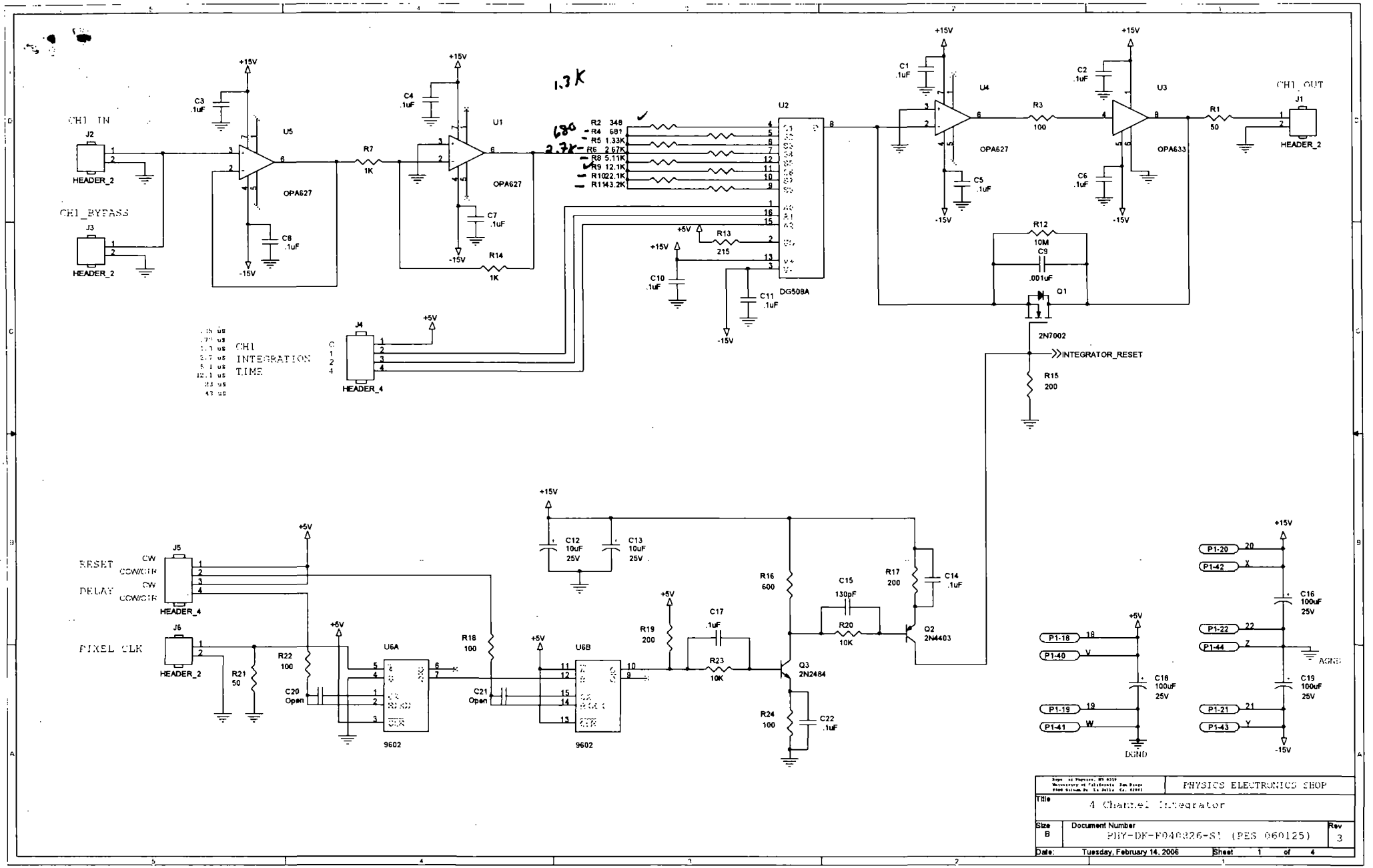
4403 9/28/05

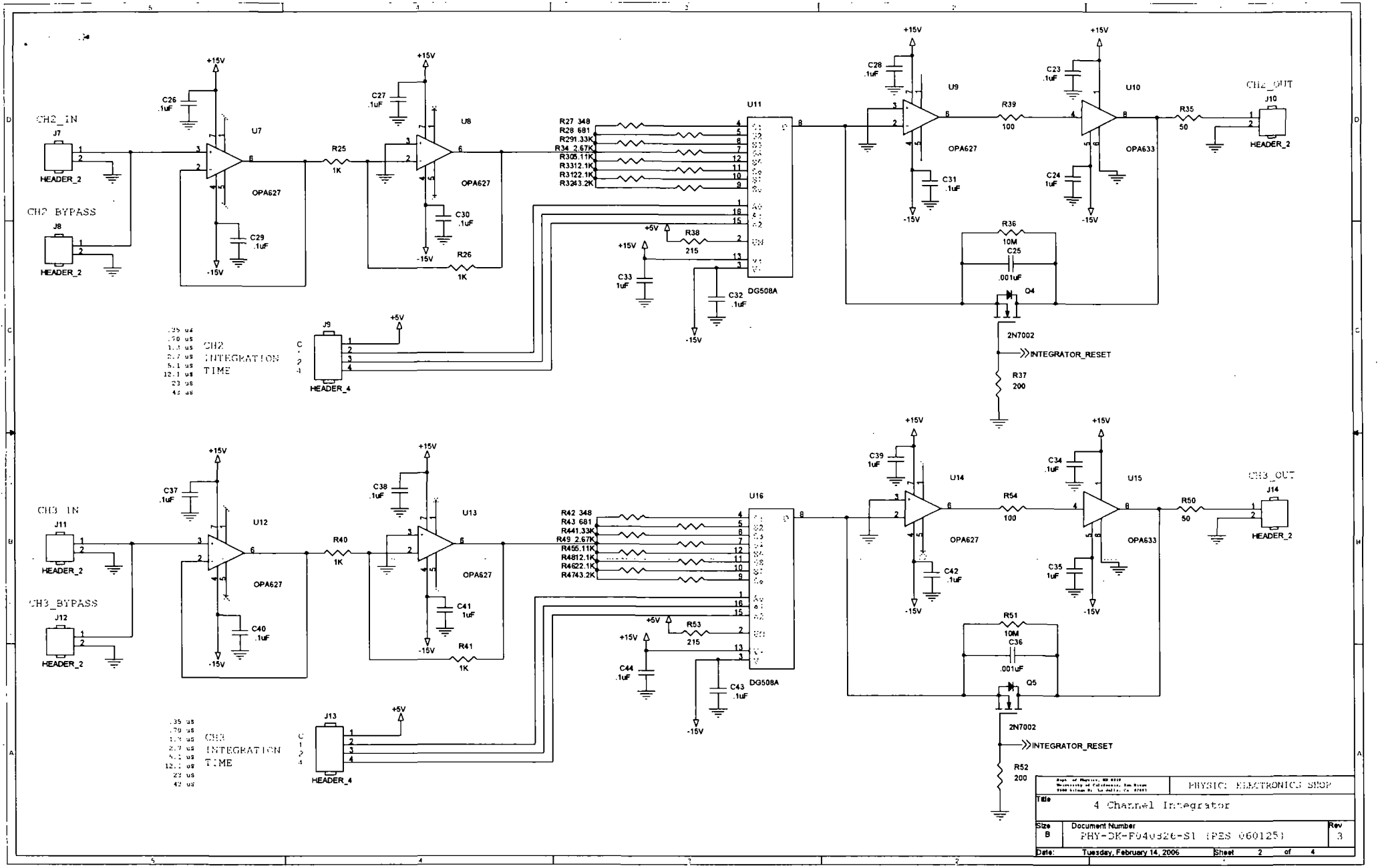

CH2_IN
J5
BNC
CH2_BYPASS
J6
BNC
U7
OPA627
U8
OPA627
C22
1uF
C23
.1uF
C25
1uF
C26
1uF
R19
1K
R20
1K
+15V
-15V
U11
DG508A
R21 348
R22 681
R23 1.33K
R28 2.67K
R24 5.11K
R27 2.1K
R25 2.1K
R26 3.2K
S1
S2
S3
S4
S5
S6
S7
S8
D
A0
A1
A2
EN
V+
V-
R31
215
+5V
C29
.1uF
C28
.1uF
U9
OPA627
U10
OPA633
C24
.1uF
C27
.1uF
C19
.1uF
C20
1uF
R32
100
R29
50
CH2_OUT
J7
BNC
R30
10M
C21
.001uF
Q2
2N7000
Q2
CH2
INTEGRATION
TIME
SW2
1_OUT
2_OUT
4_OUT
sw_1_of_8_bcd_out
P2.5
P2.6
P2.7
P2.8
INTEGRATOR_RESET
CH3_IN
J8
BNC
CH3_BYPASS
J9
BNC
U12
OPA627
U13
OPA627
C33
.1uF
C34
.1uF
C36
1uF
C37
1uF
R33
1K
R34
1K
U16
DG508A
R35 348
R36 681
R37 1.33K
R42 2.67K
R38 5.11K
R41 2.1K
R39 2.1K
R40 3.2K
R45
215
C40
.1uF
C39
1uF
U14
OPA627
U15
OPA633
C35
1uF
C38
1uF
C30
1uF
C31
.1uF
R46
100
R43
50
CH3_OUT
J10
BNC
R44
10M
C32
.001uF
Q3
2N7000
Q3
CH3
INTEGRATION
TIME
SW3
P2.9
P2.10
P2.11
P2.12
PHYSICS ELECTRONICS SHOP
Title
4 Channel Integrator
Size
B
Document Number
P030114-S1
Rev
Date
Friday, August 27, 2004
Sheet
2
of
3

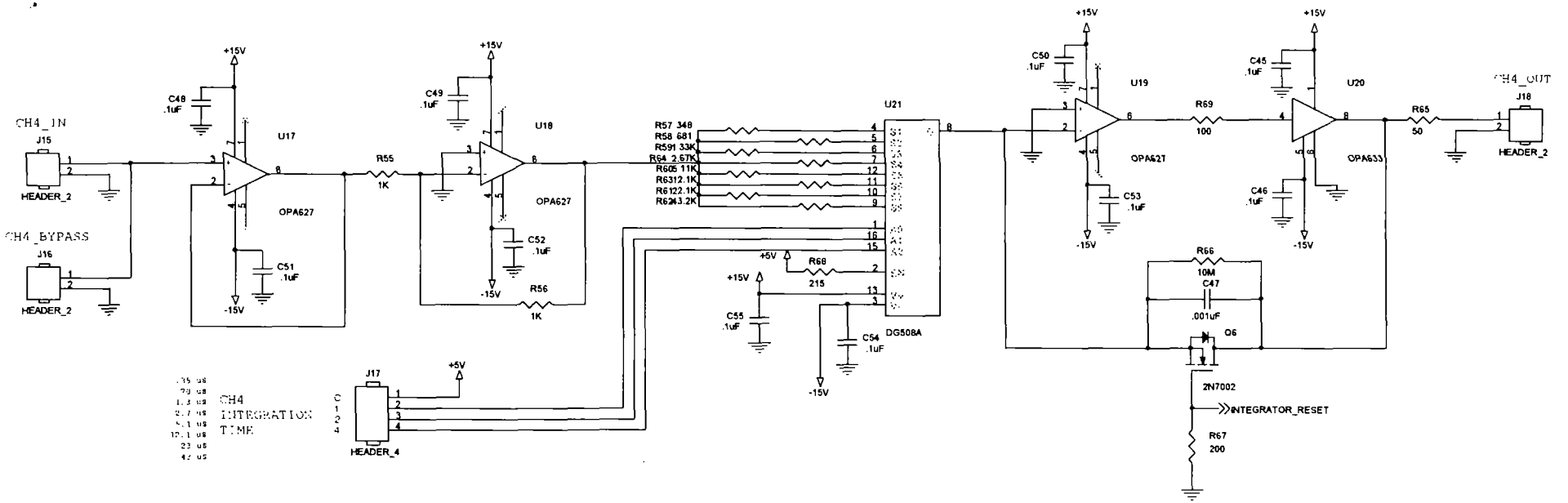


	PHYSICS ELECTRONICS SHOP
Title	4 Channel Integrator
Size B	Document Number 20020114-S1 Rev
Date	Friday, August 27, 2004 Sheet 3 of 3

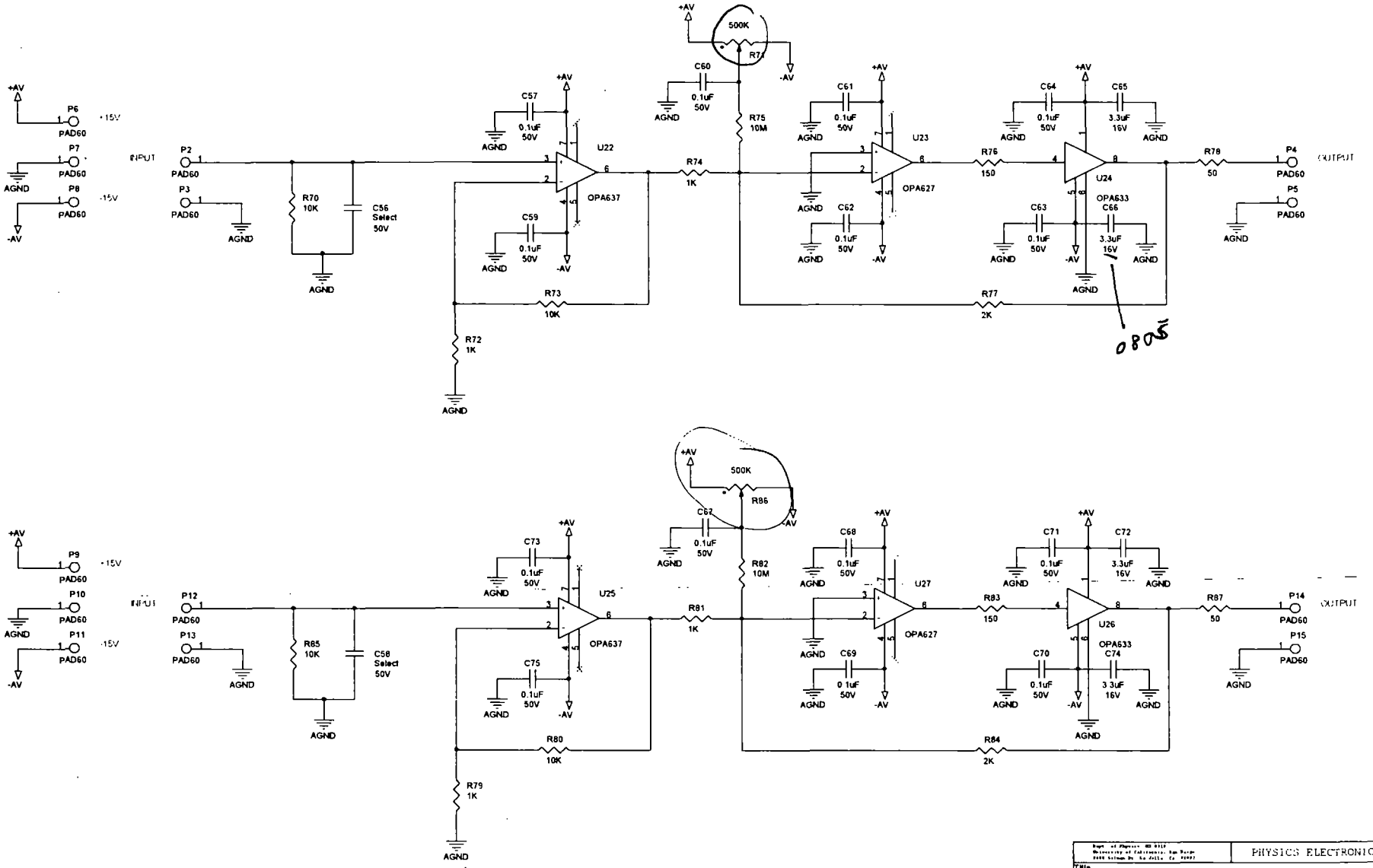



CH1 IN
CH1_BYPASS
CH1 INTEGRATION TIME
RESET
DELAY
PIXEL CLK
CW
CCW/CTR
HEADER_2
HEADER_4
OPA627
OPA633
DG508A
9602
2N7002
2N4403
2N2484
INTEGRATOR_RESET
CH1_OUT
AGND
DGND
+15V
-15V
+5V
1.3K
680
2.7K
PHYSICS ELECTRONICS SHOP
4 Channel Integrator
PHY-DE-F040326-S1 (PES 060125)
Rev 3
Tuesday, February 14, 2006
Sheet 1 of 4


CH2_IN
J7
HEADER_2
CH2 BYPASS
J8
HEADER_2
U7
OPA627
C26 .1uF
C29 .1uF
R25 1K
U8
OPA627
C27 .1uF
C30 .1uF
R26 1K
+15V
-15V
U11
DG508A
R27 348
R28 681
R291.33K
R34 2.67K
R305.11K
R3312.1K
R3122.1K
R3243.2K
R38 215
C33 1uF
C32 .1uF
+5V
U9
OPA627
C28 .1uF
C31 .1uF
R39 100
U10
OPA633
C23 .1uF
C24 1uF
R35 50
CH2_OUT
J10
HEADER_2
R36 10M
C25 .001uF
Q4
2N7002
INTEGRATOR_RESET
R37 200
J9
HEADER_4
CH2 INTEGRATION TIME
CH3_IN
J11
HEADER_2
CH3_BYPASS
J12
HEADER_2
U12
OPA627
C37 .1uF
C40 .1uF
R40 1K
U13
OPA627
C38 .1uF
C41 1uF
R41 1K
U16
DG508A
R42 348
R43 681
R441.33K
R49 2.67K
R455.11K
R4812.1K
R4622.1K
R4743.2K
R53 215
C44 .1uF
C43 .1uF
U14
OPA627
C39 1uF
C42 .1uF
R54 100
U15
OPA633
C34 .1uF
C35 1uF
R50 50
CH3_OUT
J14
HEADER_2
R51 10M
C36 .001uF
Q5
2N7002
INTEGRATOR_RESET
R52 200
J13
HEADER_4
CH3 INTEGRATION TIME
PHYSIC ELECTRONICS SHOP
Title
4 Channel Integrator
Size B
Document Number
PHY-SK-F04u320-S1 (PES 060125)
Rev 3
Date: Tuesday, February 14, 2006
Sheet 2 of 4



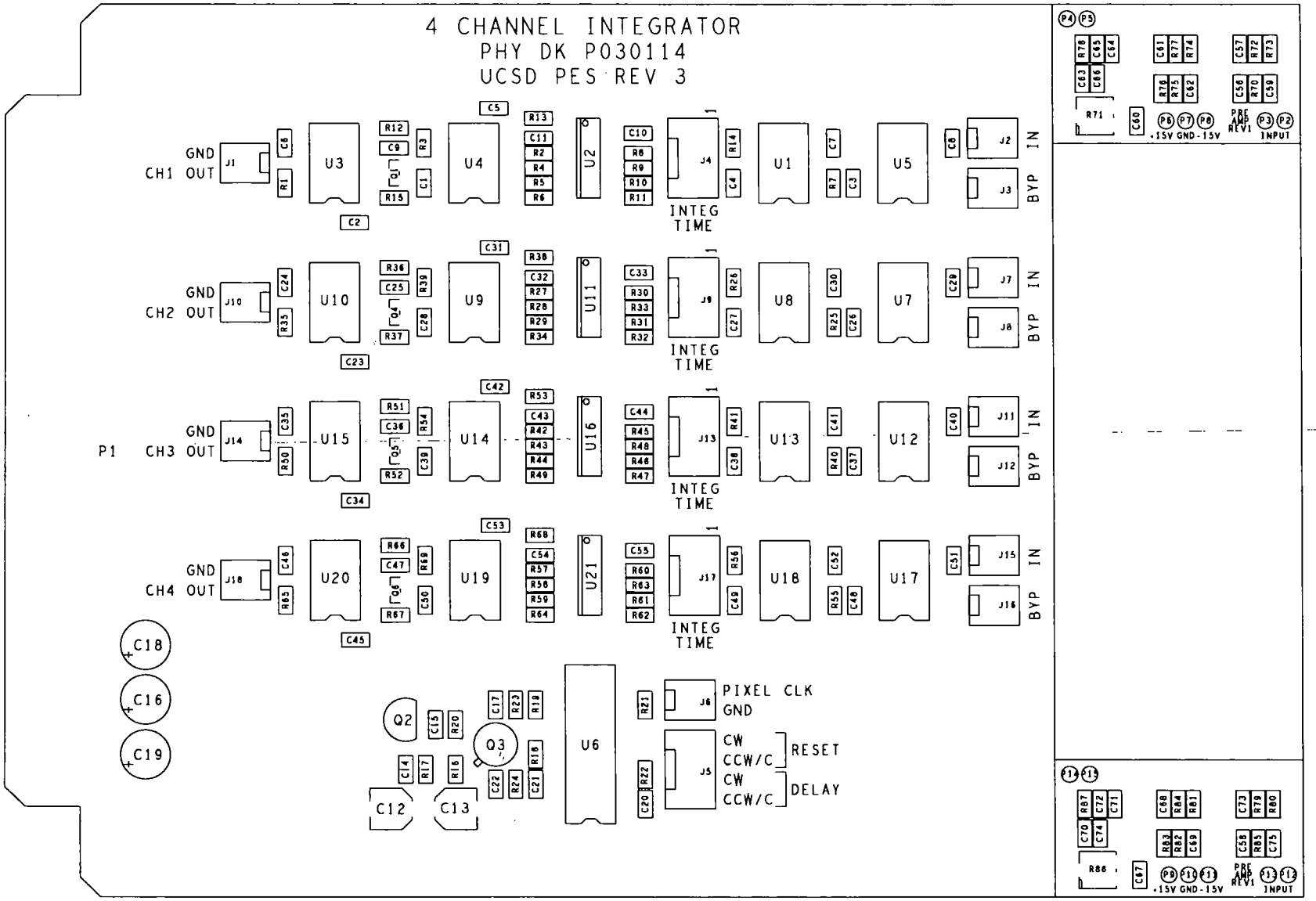
	PHYSICS ELECTRONICS SHOP	
Title	4 Channel Integrator	
Size B	Document Number PHY-DX-F040826-S1 (PES 060129)	Rev 3
Date	Tuesday, February 14, 2006	Sheet 3 of 4

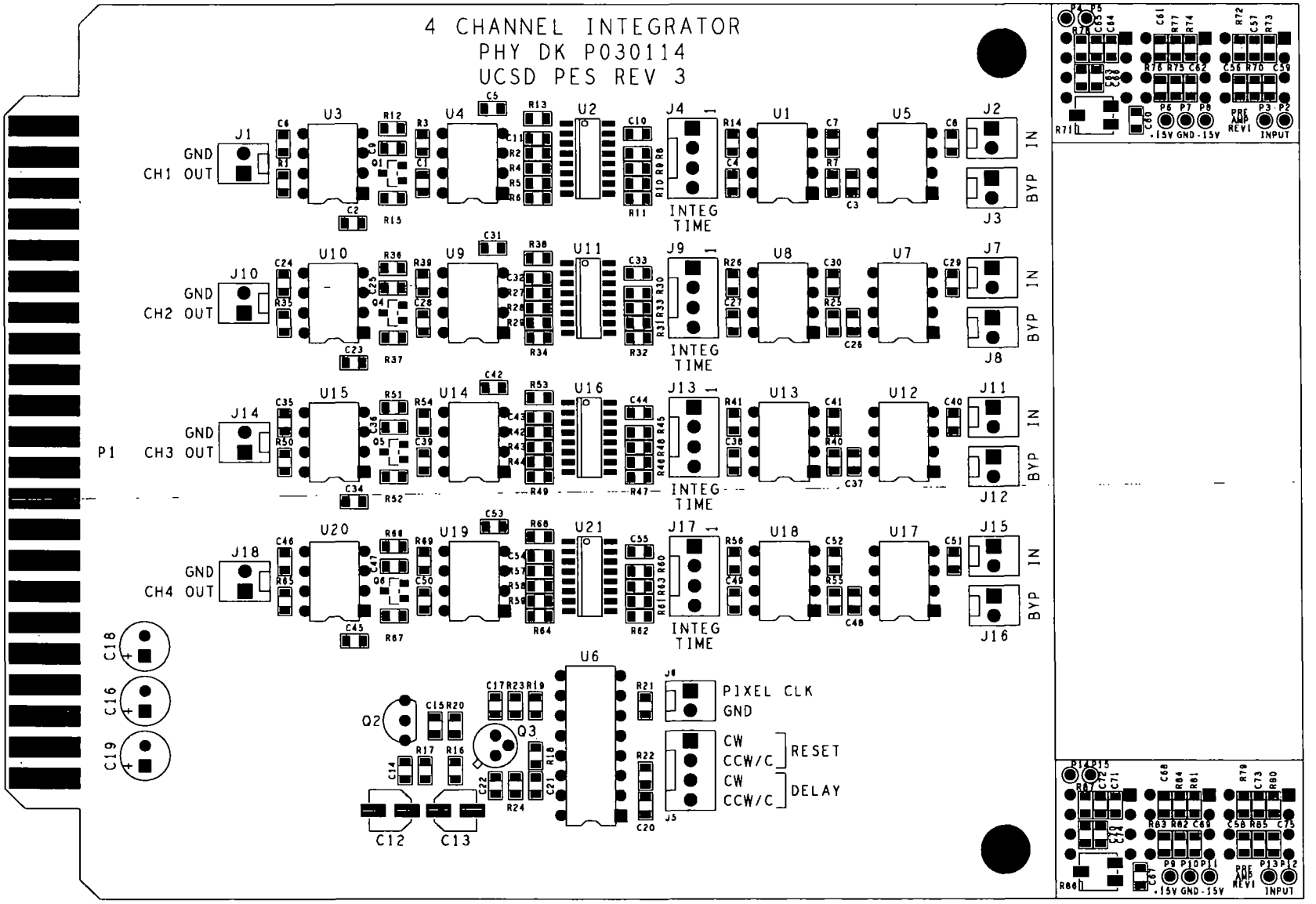


	PHYSICS ELECTRONICS SHOP
Title	PREAMP CIRCUIT
Size: B	Document Number: PHY-DK-F040826-S4 (PES 060125) — Rev: 3
Date: Thursday, February 16, 2006	Sheet 4 of 4

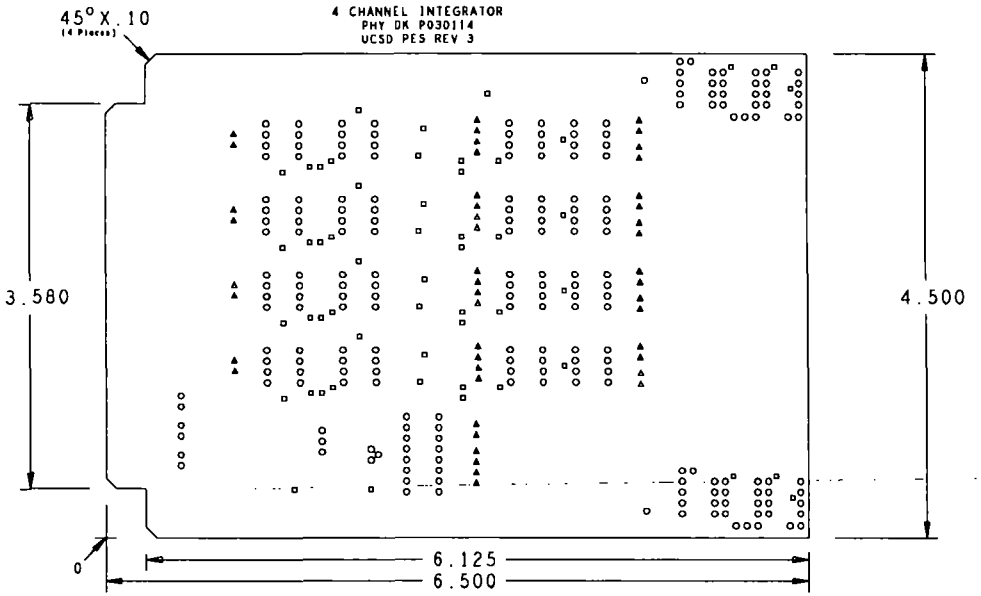
PBG5H 490-2691-6

4 CHANNEL INTEGRATOR
PHY DK P030114
UCSD PES REV 3




4 CHANNEL INTEGRATOR
PHY DK P030114
UCSD PES REV 3
P1
CH1 GND OUT
CH2 GND OUT
CH3 GND OUT
CH4 GND OUT
INTEG TIME
BYP IN
PIXEL CLK
GND
CW
CCW/C
RESET
DELAY
C18
C16
C19
C12
C13
.15V GND -15V
INPUT

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
▫	22.0	PLATED	53
○	35.0	PLATED	218
△	40.0	PLATED	46
○	120.0	PLATED	2

1. ALL LAYERS ARE VIEWED FROM COMP SIDE
2. HOLE DIAMETER IS AFTER PLATING
3. TYPE FR4 MATERIAL WITH 1 Oz. COPPER LAYERS
4. FINISHED BOARD THICKNESS 0.062 INCH
5. SILK SCREEN COMP SIDE USING WHITE EPOXY INK
6. FINISH: SOLDER PLATED
7. SOLDER MASK BOTH SIDES WITH LIQUID PHOTO IMAGEABLE MASK COLOR GREEN OVER BARE COPPER
8. EDGE CONNECTOR GOLD PLATED & BEVELED

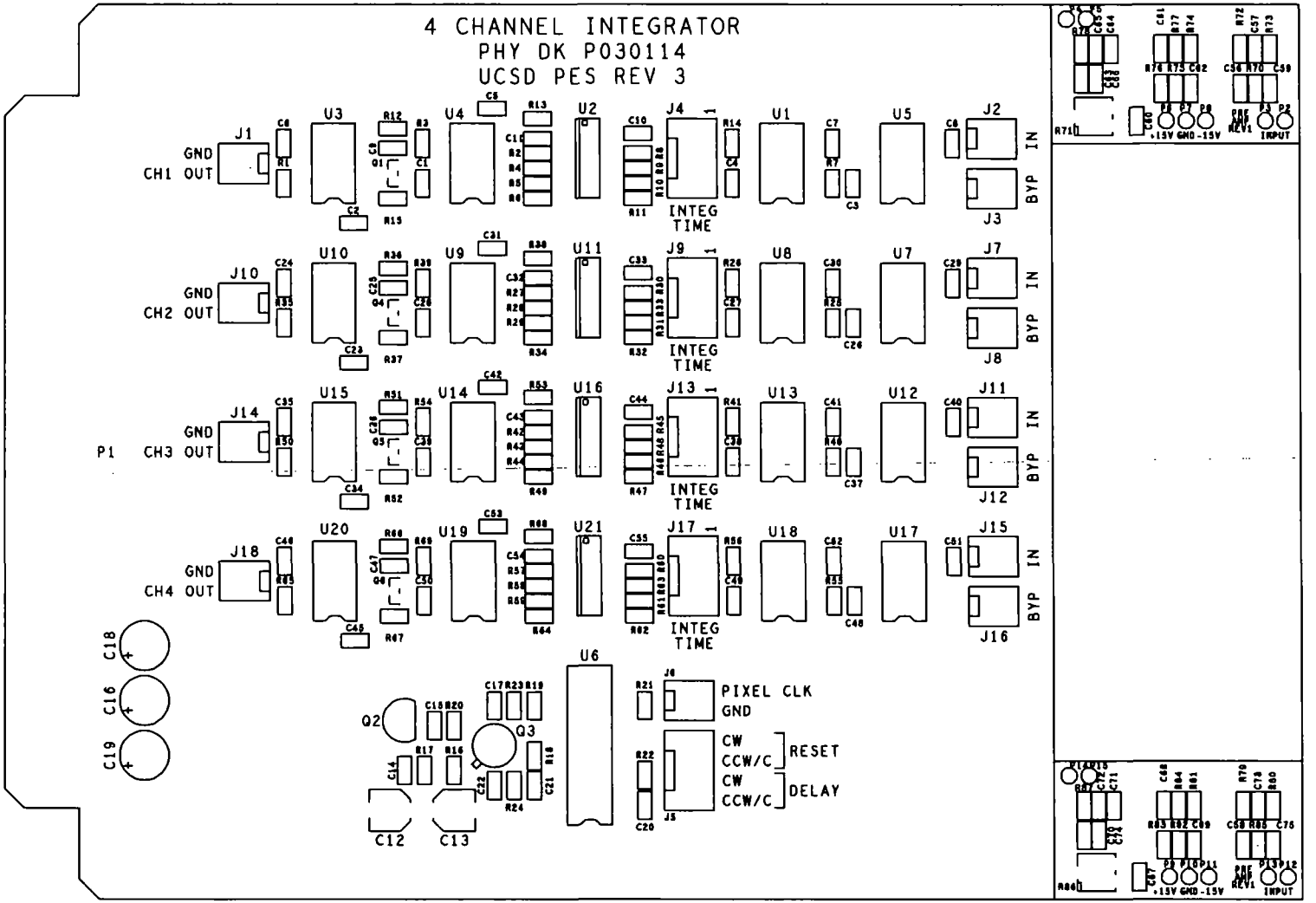
UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN INCHES TOLERANCES ON: 2 PL DECIMALS ± 3 PL DECIMALS ± ANGLES ± FRACTIONS ±		

UCSD PHYSICS DEPARTMENT

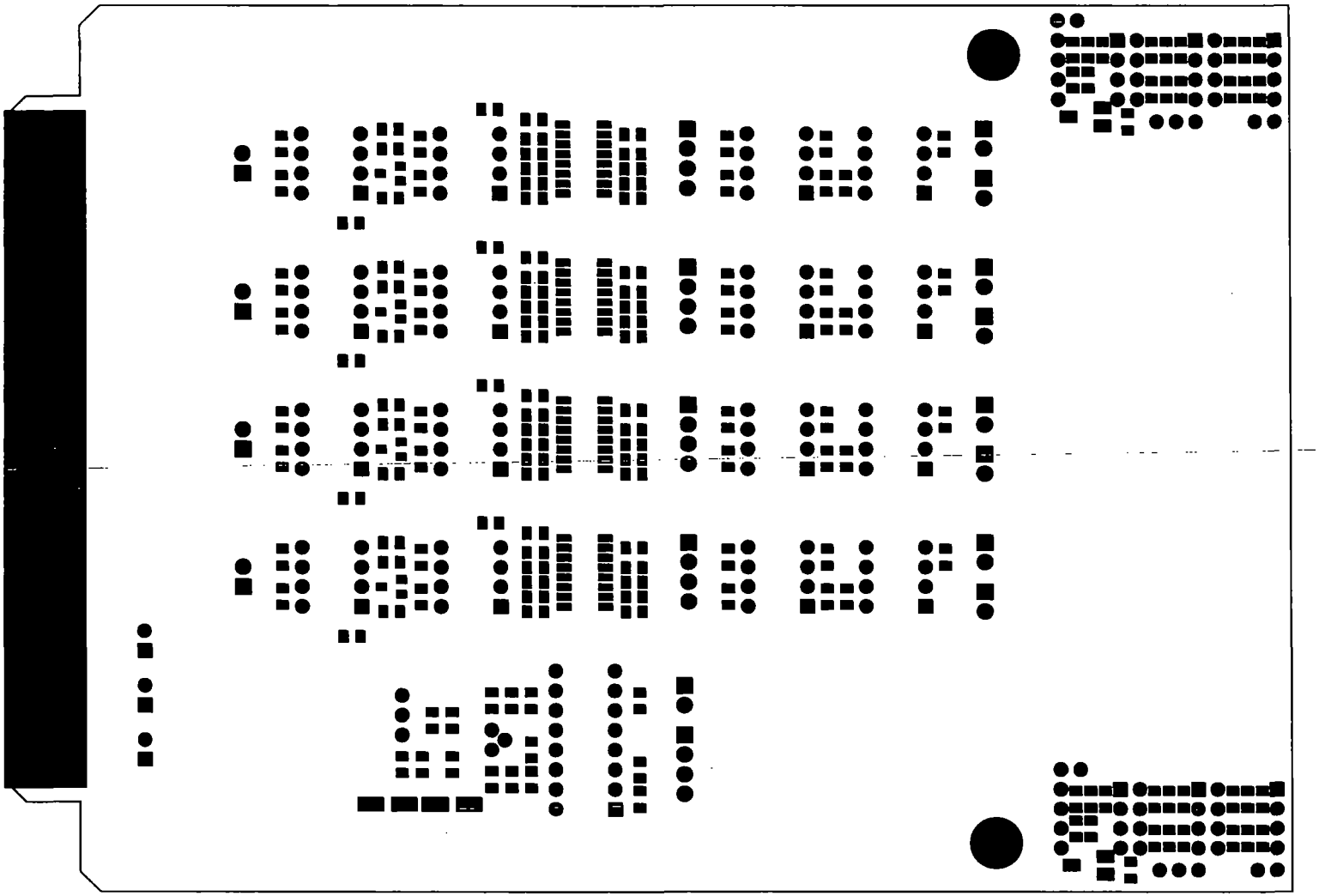
4 CHANNEL INTEGRATOR
WITH SELECTABLE GAIN/OFFSET

SIZE	FSCM NO	DWG NO
		PHY-DK-P030114-S1
SCALE		SHEET 1 OF 1

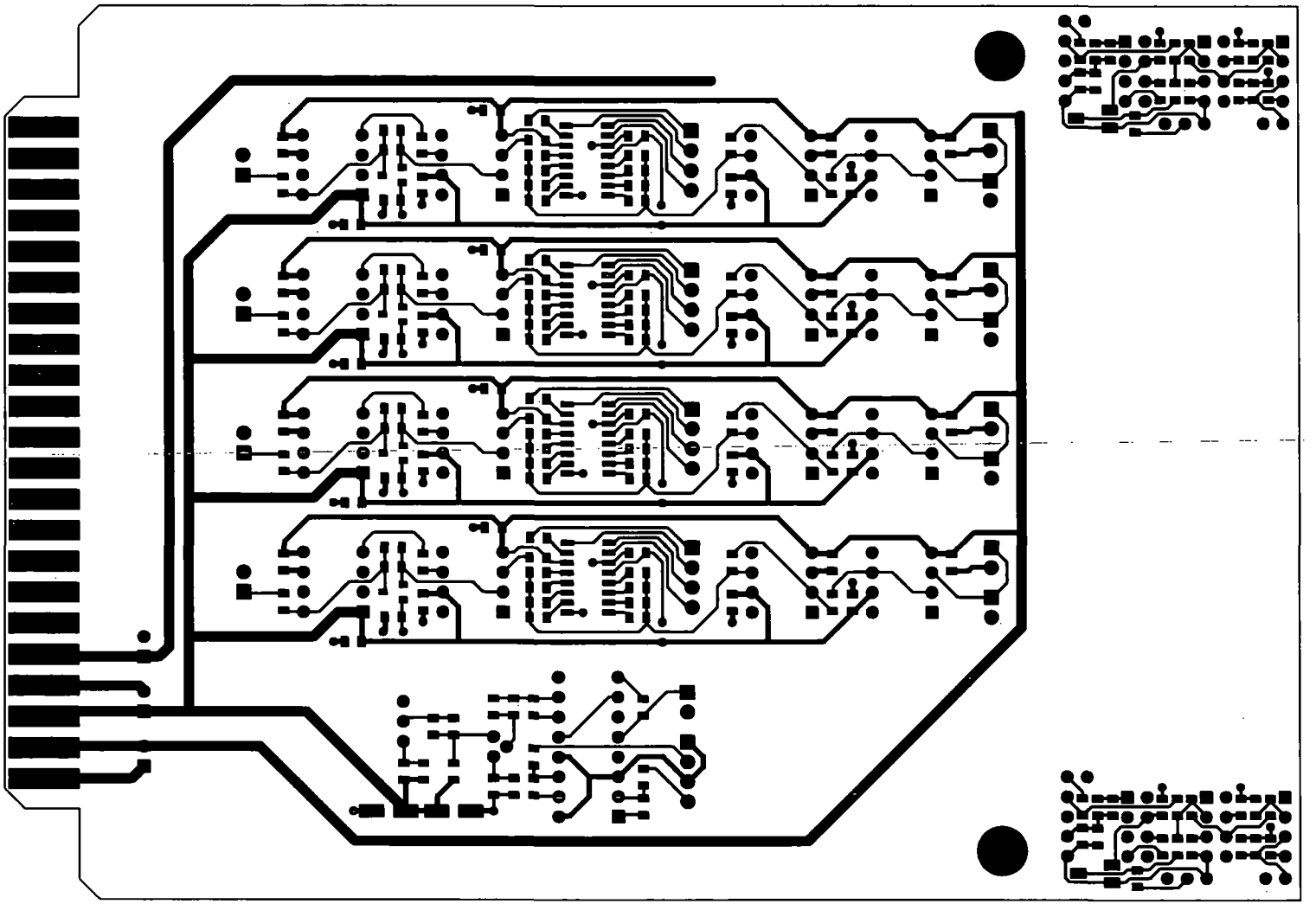
4 CHANNEL INTEGRATOR
PHY DK P030114
UCSD PES REV 3



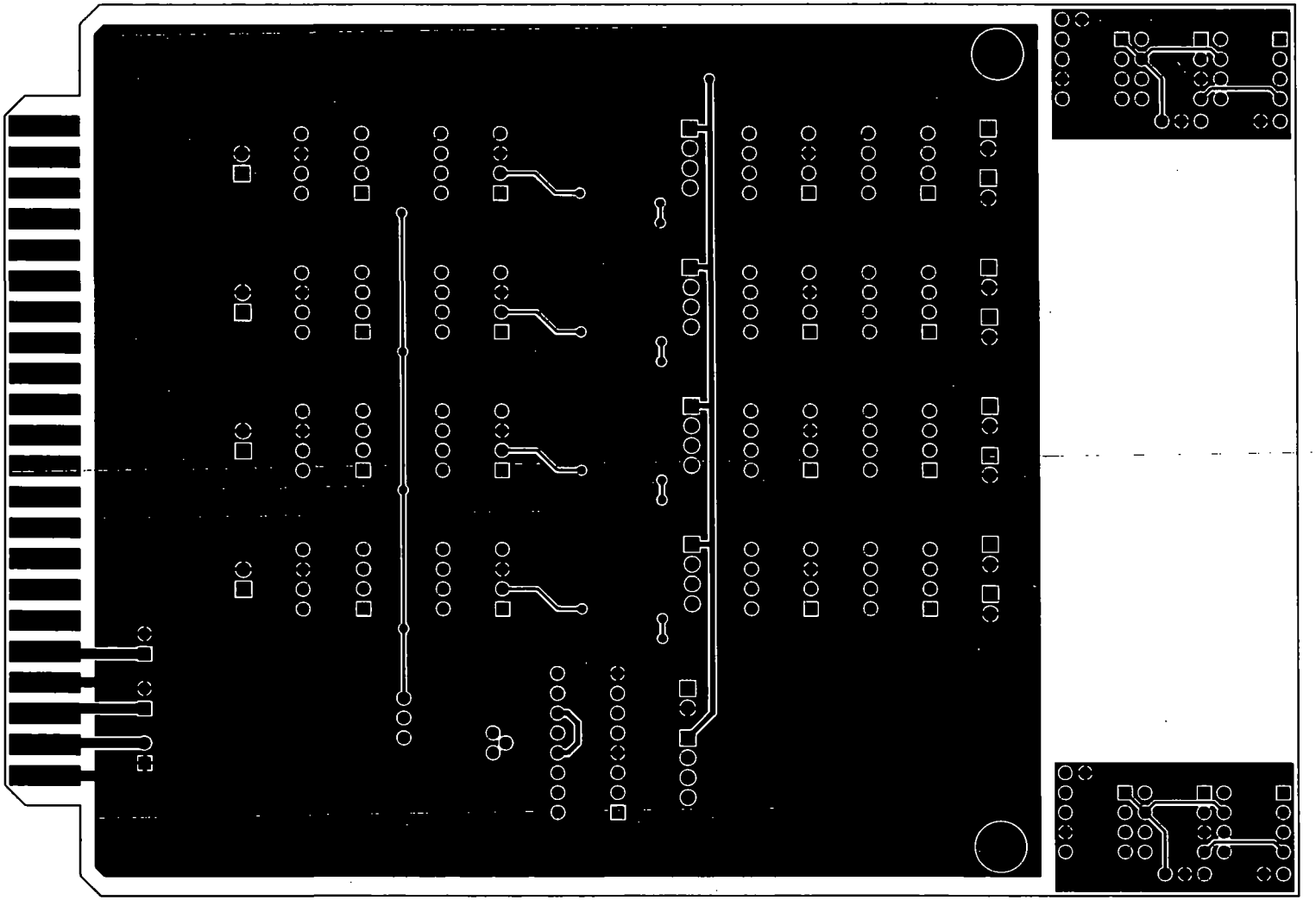
4 CHANNEL INTEGRATOR
PHY DK P030114
UCSD PES REV 3



4 CHANNEL INTEGRATOR
PHY DK P030114
UCSD PES REV 3



4 CHANNEL INTEGRATOR
PHY DK P030114
UCSD PES REV 3



4 CHANNEL INTEGRATOR
PHY DK P030114
UCSD PES REV 3