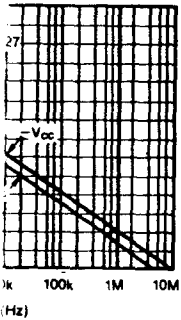
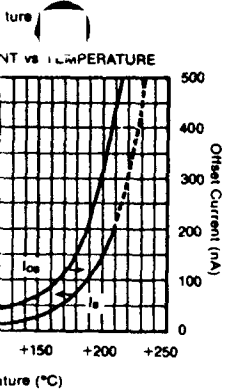
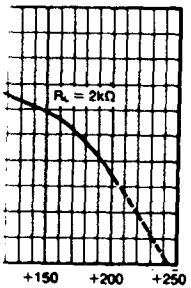


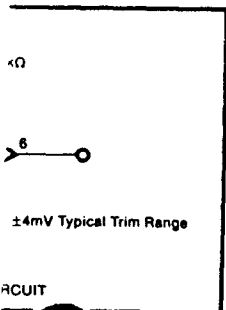
ON vs FREQUENCY



N vs TEMPERATURE



n for 28 hours at +200°C



OPA101  
OPA102

## Low Noise - Wideband PRECISION JFET INPUT OPERATIONAL AMPLIFIER

### FEATURES

- GUARANTEED NOISE SPECTRAL DENSITY - 100% Tested
- LOW VOLTAGE NOISE -  $8nV/\sqrt{Hz}$  max at 10kHz
- LOW VOLTAGE DRIFT -  $5\mu V/^\circ C$  max (B grade)
- LOW OFFSET VOLTAGE -  $250\mu V$  max (B grade)
- LOW BIAS CURRENTS - 10pA max at 25°C Ambient (B Grade)
- HIGH SPEED -  $10V/\mu sec$  min (OPA102)
- GAIN BANDWIDTH PRODUCT - 40MHz (OPA102)

### APPLICATIONS

- LOW NOISE SIGNAL CONDITIONING
- LIGHT MEASUREMENTS
- RADIATION MEASUREMENTS
- PIN DIODE APPLICATIONS
- DENSITOMETERS
- PHOTODIODE/PHOTOMULTIPLIER CIRCUITS
- LOW NOISE DATA ACQUISITION

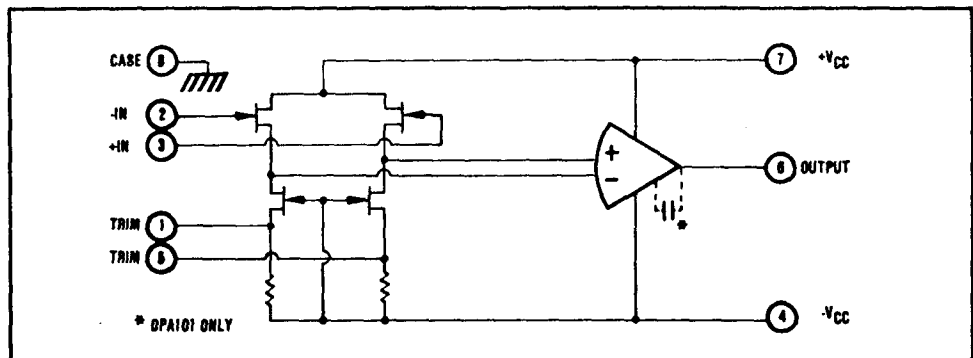
### DESCRIPTION

The OPA101 and OPA102 are the first FET operational amplifiers available with noise characteristics (voltage spectral density) guaranteed and 100% tested.

The amplifiers have a complementary set of specifications permitting low errors in signal conditioning applications; low noise, low bias current, high open-loop gain, high common-mode rejection, low offset voltage, low offset voltage drift, etc.

In addition, the amplifiers have moderately high speed. The OPA101 is compensated for unity gain stability and has a slew rate of  $5V/\mu sec$ , min. The OPA102 is compensated for gains of  $3V/V$  and above and has a slew rate of  $10V/\mu sec$ , min.

Each unit is laser-trimmed for low offset voltage and low offset voltage drift versus temperature. Bias currents are specified with the units fully warmed up at +25°C ambient temperature.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6401

PDS-434B

# SPECIFICATIONS

## ELECTRICAL

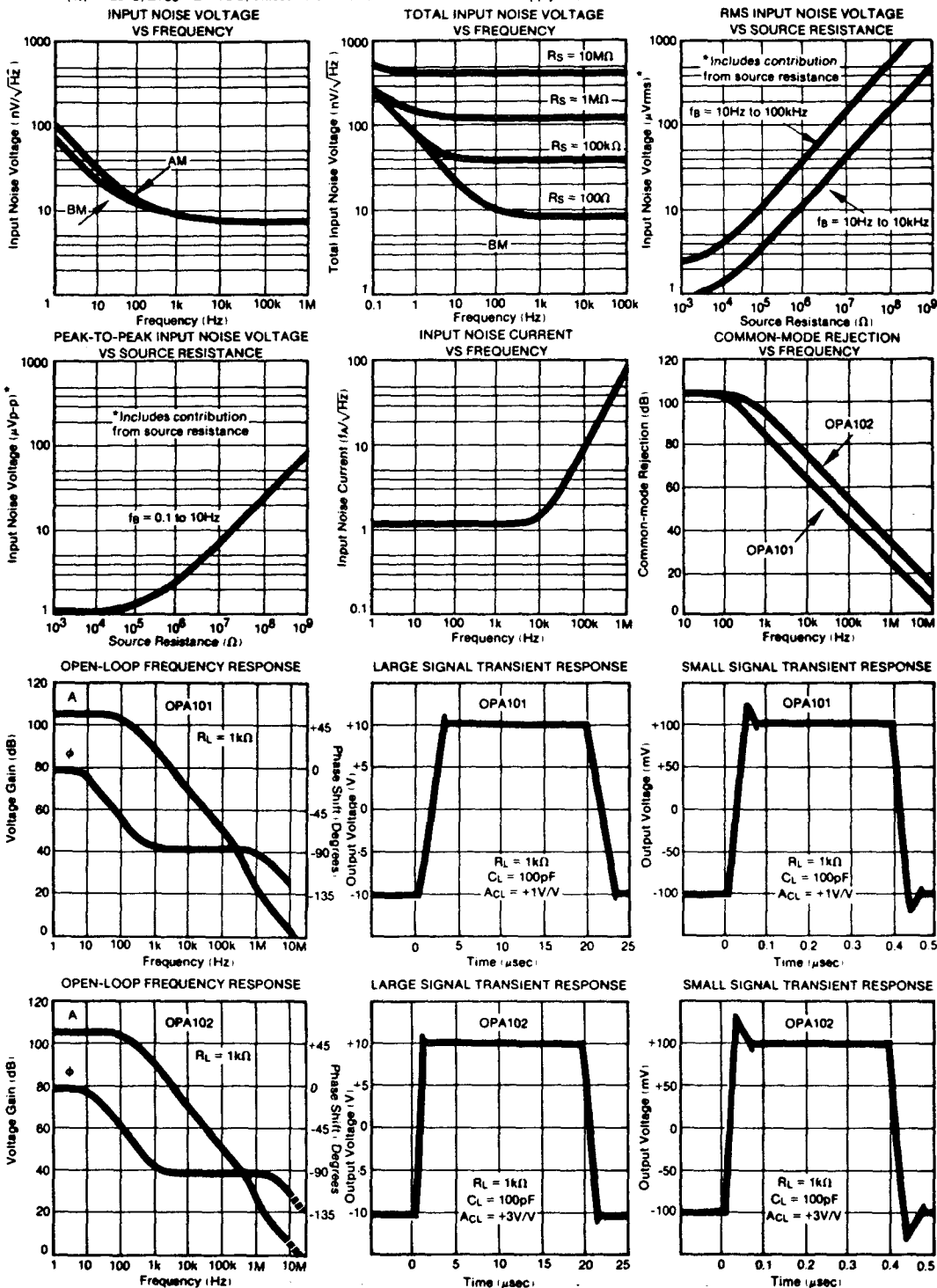
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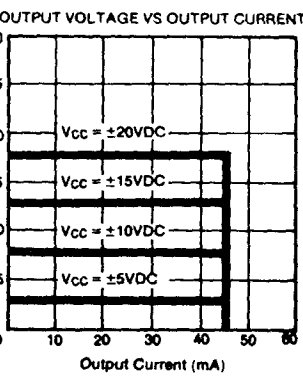
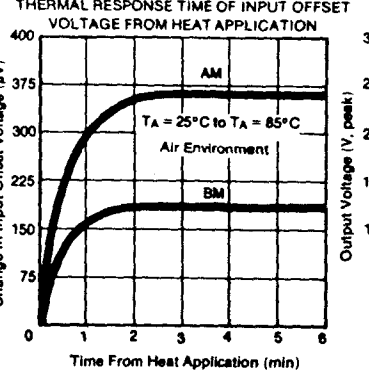
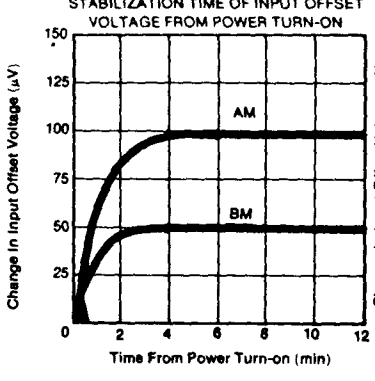
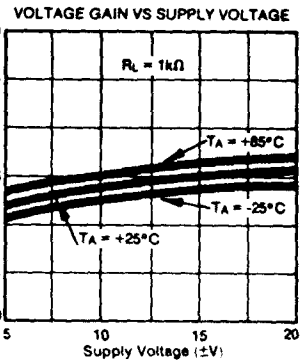
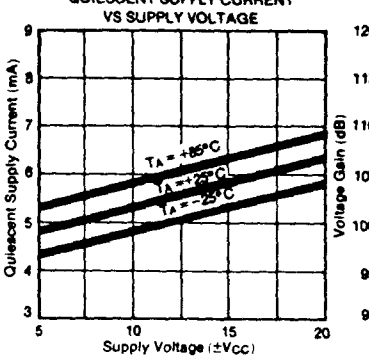
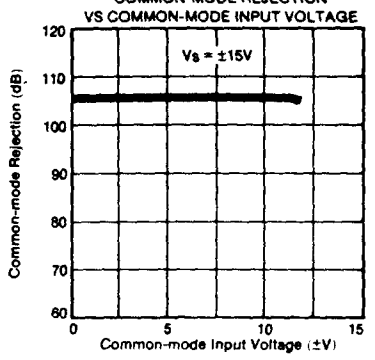
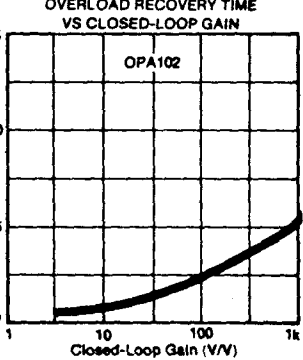
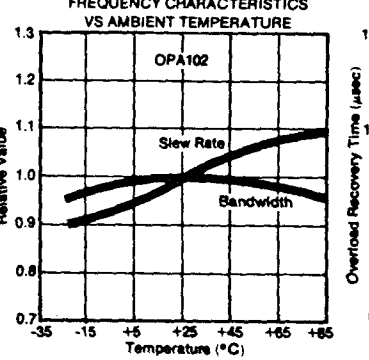
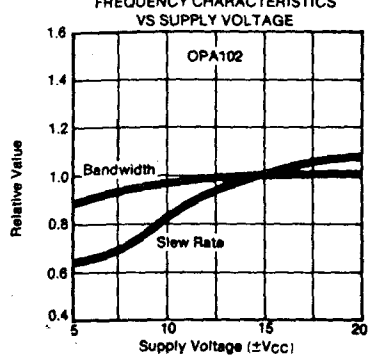
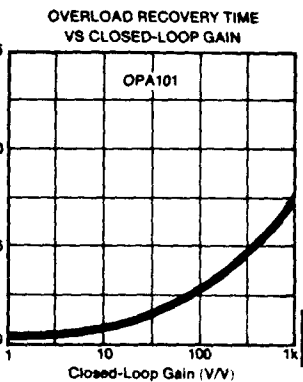
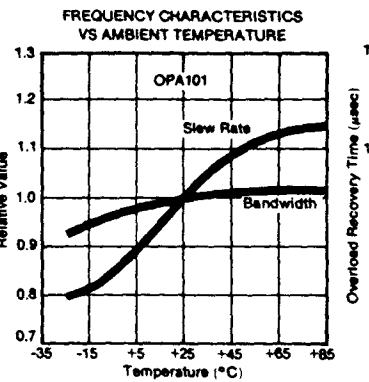
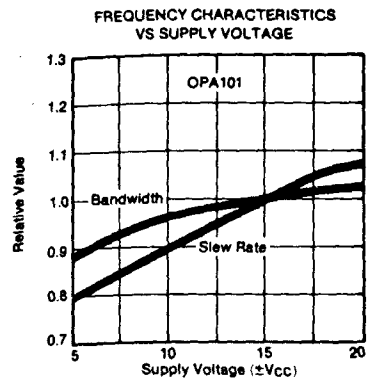
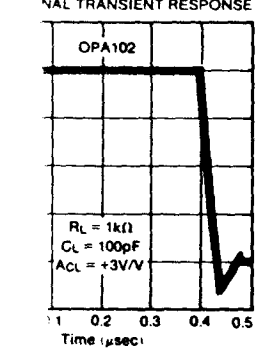
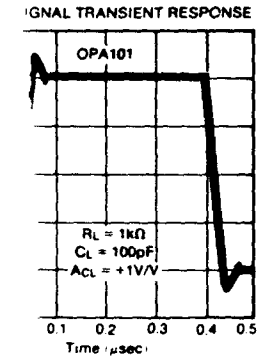
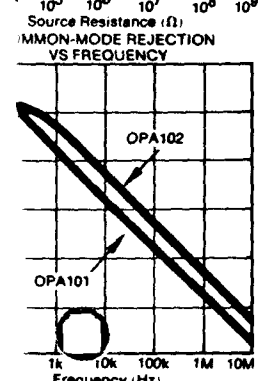
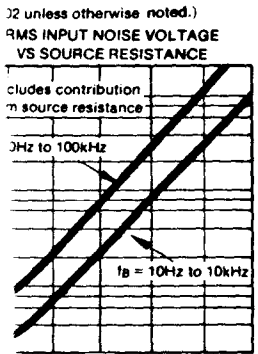
MODEL	PARAMETER	CONDITION	OPA101/102AM			OPA101/102SM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT NOISE</b>									
Voltage Noise Density		$f_o = 1\text{Hz}^{(1)}$		100	200		80	100	$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 10\text{Hz}$		32	60		25	30	$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 100\text{Hz}$		14	30		11	15	$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 1\text{kHz}$		9	15		8	12	$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 10\text{kHz}$		7	8		7	8	$\text{nV}/\sqrt{\text{Hz}}$
		$f_o = 100\text{kHz}$		6.5	8		6.5	8	$\text{nV}/\sqrt{\text{Hz}}$
$f_c$ : 1/1 Corner Frequency			125			100		Hz	
Voltage Noise		$f_b = 0.1\text{Hz}$ to $10\text{Hz}^{(1)}$		1.3	2.6		1.0	1.3	$\mu\text{V}$ , p-p
		$f_b = 10\text{Hz}$ to $10\text{kHz}$		1.0	1.2		0.8	1.0	$\mu\text{V}$ , rms
		$f_b = 10\text{Hz}$ to $100\text{kHz}$		2.1	2.6		2.1	2.6	$\mu\text{V}$ , rms
Current Noise Density		$f_o = 0.1\text{Hz}$ thru $10\text{kHz}$		2.0			1.4		$\text{fA}/\sqrt{\text{Hz}}$
		$f_b = 0.1\text{Hz}$ to $10\text{Hz}$		38			26		$\text{fA}$ , p-p
Current Noise		$f_b = 10\text{Hz}$ to $10\text{kHz}$		200			140		$\text{fA}$ , rms
<b>DYNAMIC RESPONSE</b>									
Bandwidth, Unity Gain		Small Signal		10					MHz
OPA101				Note 2					
OPA102									
Gain-Bandwidth Product		$A_{CL} = 100$		20					MHz
OPA101				40					MHz
OPA102									
Full Power Bandwidth		$V_o = 20\text{V}$ , p-p; $R_L = 1\text{k}\Omega$							
OPA101			80	100					kHz
OPA102			160	210					kHz
Slew Rate		$V_o = \pm 10\text{V}$ ; $R_L = 1\text{k}\Omega$							
OPA101		$A_{CL} = -1$	5	6.5					$\text{V}/\mu\text{sec}$
OPA102		$A_{CL} = -3$	10	14					$\text{V}/\mu\text{sec}$
Settling Time (OPA101)		$V_o = \pm 5\text{V}$ ; $A_{CL} = -1$ ; $R_L = 1\text{k}\Omega$							
$\epsilon = 1\%$				2					$\mu\text{sec}$
$\epsilon = 0.1\%$				2.5					$\mu\text{sec}$
$\epsilon = 0.01\%$				10					$\mu\text{sec}$
Settling Time (OPA102)		$V_o = \pm 5\text{V}$ ; $A_{CL} = -3$ ; $R_L = 1\text{k}\Omega$							
$\epsilon = 1\%$				1					$\mu\text{sec}$
$\epsilon = 0.1\%$				1.5					$\mu\text{sec}$
$\epsilon = 0.01\%$				8					$\mu\text{sec}$
Small-Signal Overshoot		$R_L = 1\text{k}\Omega$ ; $C_L = 100\text{pF}$							
OPA101		$A_{CL} = +1$		15					%
OPA102		$A_{CL} = +3$		20					%
Rise Time		10% to 90%, Small Signal							
OPA101				40					nsec
OPA102				30					nsec
Phase Margin		$R_L = 1\text{k}\Omega$							
OPA101		$A_{CL} = +1$		60					Degrees
OPA102		$A_{CL} = +3$		45					Degrees
Overload Recovery <sup>(3)</sup>									
OPA101		$A_{CL} = -1$ , 50% overdrive		1					$\mu\text{sec}$
OPA102		$A_{CL} = -3$ , 50% overdrive		0.8					$\mu\text{sec}$
<b>OPEN-LOOP GAIN, DC</b>									
Full Load		$V_o = \pm 10\text{V}$ ; $R_L = 1\text{k}\Omega$	94	105					dB
No Load		$V_o = \pm 10\text{V}$ ; $R_L \geq 10\text{k}\Omega$	96	108					dB
<b>RATED OUTPUT</b>									
Voltage		$I_o = \pm 12\text{mA}$	$\pm 12$	$\pm 13$					V
Current		$V_o = \pm 12\text{V}$	$\pm 12$	$\pm 30$					mA
Output Resistance		Open-Loop, $f = \text{DC}$		500					$\Omega$
Short-Circuit Current				$\pm 45$					mA
Capacitive Load Range		Phase Margin $\geq 25^\circ$							
OPA101		$A_{CL} = +1$		500					pF
OPA102		$A_{CL} = +3$		300					pF
<b>INPUT OFFSET VOLTAGE</b>									
Initial Offset		$T_A = +25^\circ\text{C}$		$\pm 100$	$\pm 500$		$\pm 50$	$\pm 250$	$\mu\text{V}$
vs Temperature		$-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		$\pm 6$	$\pm 10$		$\pm 3$	$\pm 5$	$\mu\text{V}/^\circ\text{C}$
vs Supply Voltage		$\pm 5\text{VDC} \leq  V_{CC}  \leq \pm 20\text{VDC}$		$\pm 10$	$\pm 50$				$\mu\text{V}/\text{V}$
vs Time				$\pm 10$					$\mu\text{V}/\text{mo.}$
Adjustment Range		Circuit in "Connection Diagram"		$\pm 1$					mV
<b>INPUT BIAS CURRENT</b>									
Initial Bias		$T_A = +25^\circ\text{C}$		-12	-15		-6	-10	pA
vs Temperature				Note 4					
vs Supply Voltage				Note 5					

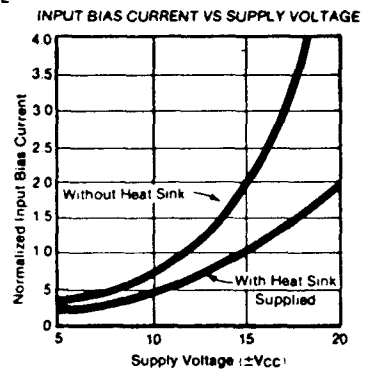
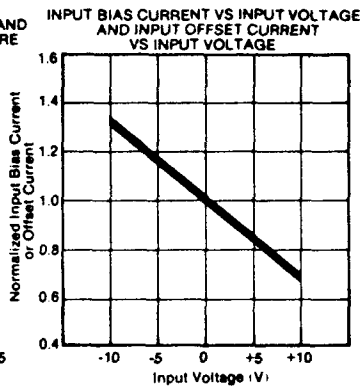
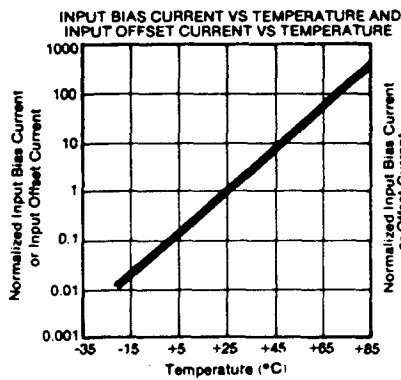
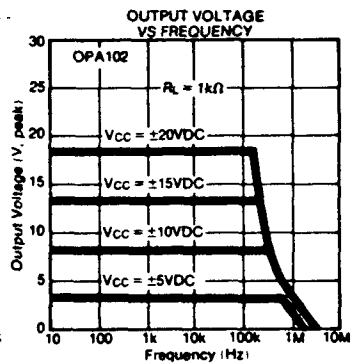
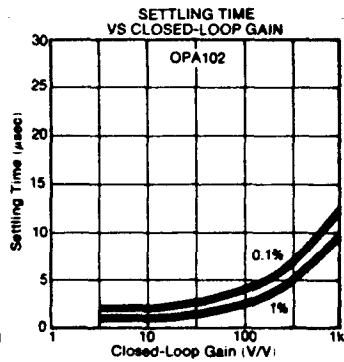
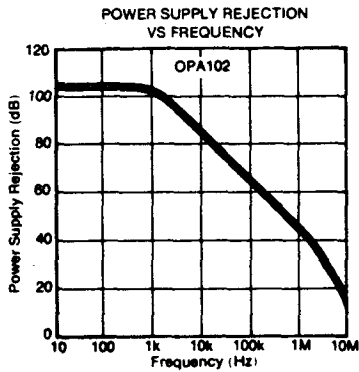
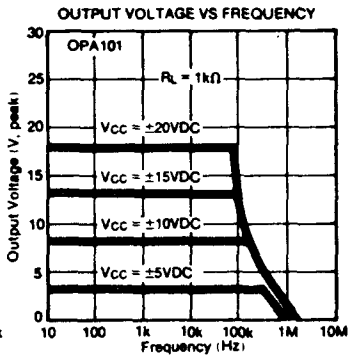
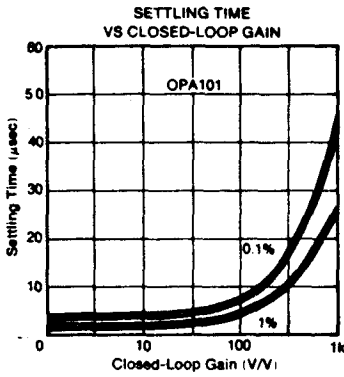
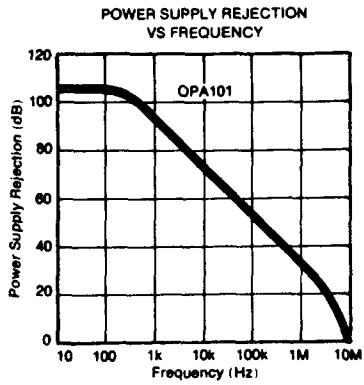


# TYPICAL PERFORMANCE CURVES

( $T_A = +25^\circ\text{C}$ ,  $\pm V_{CC} = \pm 15\text{VDC}$ , unless otherwise noted. Performance curves apply to both OPA101 and OPA102 unless otherwise noted.)







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## APPLICATION INFORMATION

### INTRODUCTION

The availability of detailed noise spectral density characteristics for the OPA101/102 amplifiers allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

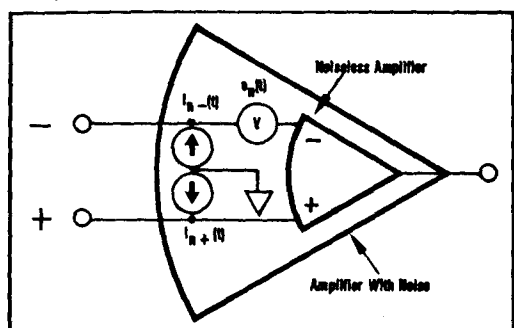


FIGURE 1. Noise Model of OPA101/102.

Noise in the OPA101/102 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage ( $E_{OS}$ ) and bias currents ( $I_B$ ). In fact, if the voltage  $e_n(t)$  and currents  $i_n(t)$  are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2 below.

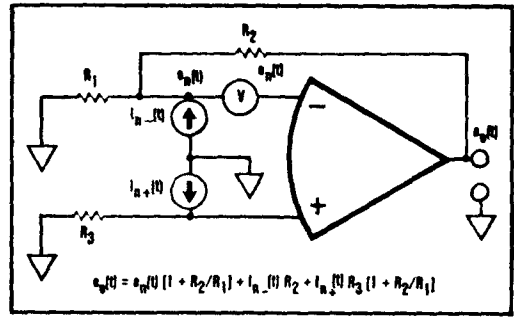


FIGURE 2. Circuit With Error Sources.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same direct way to compute noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average - most commonly the rms value.

$$N_{rms} = \sqrt{1/T \int_0^T n^2(t) dt} \quad (1)$$

where  $N_{rms}$  is the rms value of some random variable  $n(t)$ . In the case of amplifier noise,  $n(t)$  represents either  $e_n(t)$  or  $i_n(t)$ .

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if  $n_1(t)$ ,  $n_2(t)$ , and  $n_3(t)$  are uncorrelated then their combined value is

$$N_{TOTAL\ rms} = \sqrt{N_1^2\ rms + N_2^2\ rms + N_3^2\ rms} \quad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

### TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

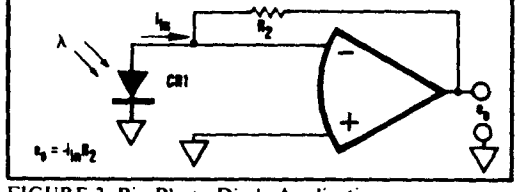


FIGURE 3. Pin Photo Diode Application.

CR1 is a PIN photo diode connected in the photovoltaic mode (no bias voltage) which produces an output current  $i_n$  when exposed to the light,  $\lambda$ .

A more complete circuit is shown in Figure 4. The values shown for  $C_1$  and  $R_1$  are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of  $C_2$  is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of  $C_2$  would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

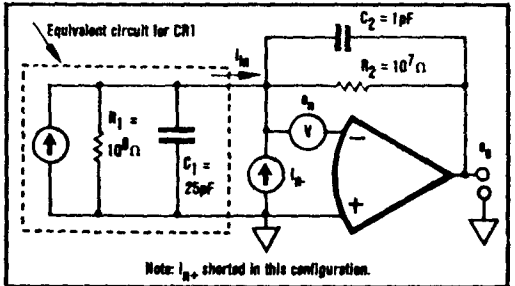
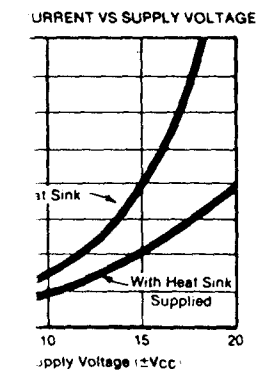
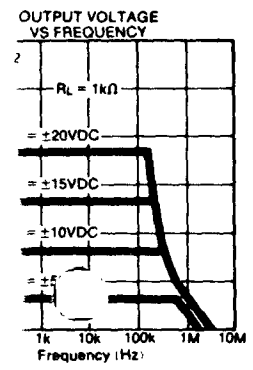
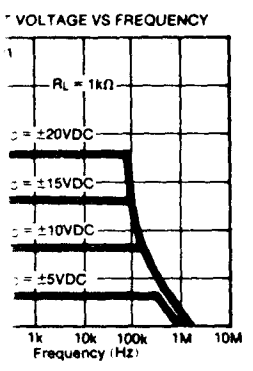


FIGURE 4. Noise Model of Photo Diode Application.



In Figure 4,  $e_n$  and  $i_n$  represent the amplifier's voltage and current spectral densities,  $e_n(\omega)$  and  $i_n(\omega)$  respectively. These are shown in Figure 5.

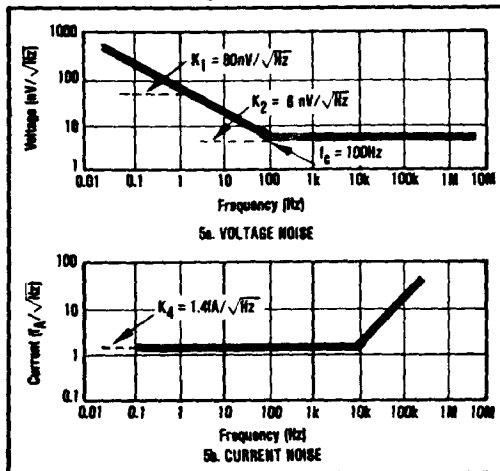


FIGURE 5. Noise Voltage and Current Spectral Density.

Figure 6 shows the desired "gain" of the circuit (transimpedance of  $e_n/i_n = Z_2(s)$ ). It has a single-pole rolloff at  $f_2 = 1/(2\pi R_2 C_2) = \omega_2/2\pi$ . Output noise is minimized if  $f_2$  is made smaller. Normally  $R_2$  is chosen for the desired DC transimpedance based on the full scale input current ( $i_n$  full scale) and maximum output ( $e_o$  max). Then  $C_2$  is chosen to make  $f_2$  as small as possible consistent with the necessary signal frequency response.

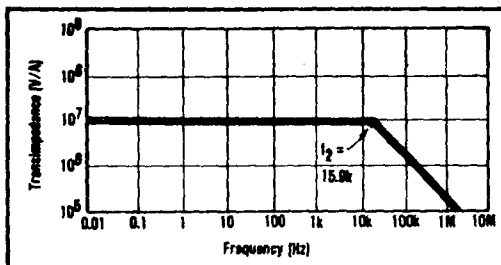


FIGURE 6. Transimpedance.

#### Voltage Noise

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_o = e_n \left[ \frac{A}{1 + A\beta} \right] = e_n \frac{1}{\beta} \left[ \frac{1}{1 + \frac{1}{A\beta}} \right] \quad (3)$$

where:

- $A = A(\omega)$  is the open-loop gain
- $\beta = \beta(\omega)$  is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.
- $A\beta = A(\omega)\beta(\omega)$  is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

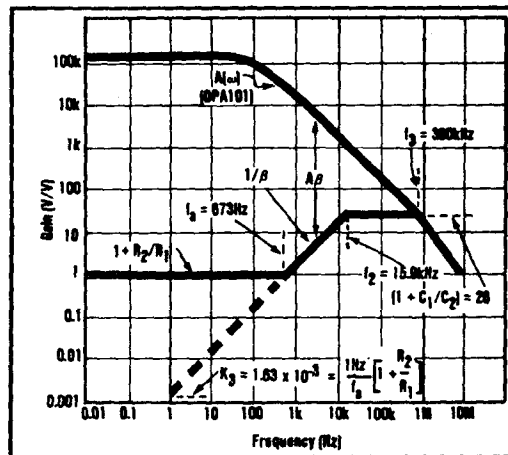


FIGURE 7. Noise Voltage Gain.

Note that for large loop gain ( $A\beta \gg 1$ )

$$e_o \approx e_n \frac{1}{\beta} \quad (4)$$

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2(R_1 C_1 s + 1)}{R_1(R_2 C_2 s + 1)} \quad (5)$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2 + R_1}{R_1} \left[ \frac{\tau_2 s + 1}{\tau_1 s + 1} \right] \quad (5a)$$

where  $\tau_1 = (R_1 \parallel R_2)(C_1 \parallel C_2)$  (5b)

$$= \left[ \frac{R_1 R_2}{R_1 + R_2} \right] (C_1 + C_2)$$

and  $\tau_2 = R_2 C_2$  (5c)

Then,  $f_1 = \frac{1}{2\pi\tau_1}$  and  $f_2 = \frac{1}{2\pi\tau_2}$  (5d)

For very low frequencies ( $f \ll f_1$ ),  $s$  approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1} \quad (6)$$

For very high frequencies ( $f \gg f_2$ ),  $s$  approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2} \quad (7)$$



The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuit's noise gain (Figure 7). Since both curves are plotted on log-log scales the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

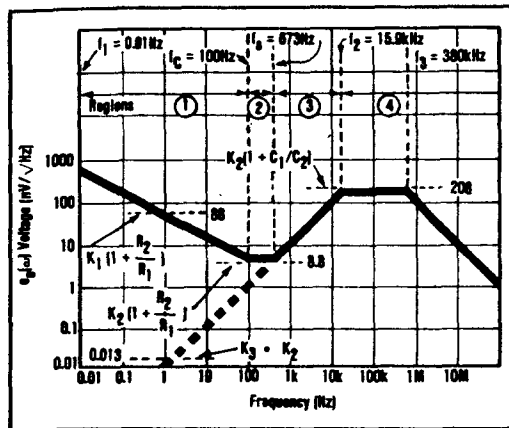


FIGURE 8. Output Noise Voltage Spectral Density. The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the  $e_o(\omega)$  function in Figure 8 with the following expression:

$$E_{o \text{ rms}} = \sqrt{\int_{-\infty}^{+\infty} e_o^2(\omega) d\omega} \quad (8)$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the four regions indicated in Figure 8.

Region 1;  $f_1 = 0.01 \text{ Hz}$  to  $f_c = 100 \text{ Hz}$

$$E_{n1 \text{ rms}} = K_1 \left(1 + \frac{R_2}{R_1}\right) \sqrt{\ln(f_c/f_1)} \quad (9)$$

$$= 80 \text{ nV}/\sqrt{\text{Hz}} \left(1 + \frac{10^7}{10^4}\right) \sqrt{\ln \frac{100}{0.01}} \quad (9a)$$

$$= 0.267 \mu\text{V}$$

This region has the characteristic of  $1/f$  or "pink" noise (slope of -10dB per decade on the log-log plot of  $e_o(\omega)$ ). The selection of 0.01 Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending  $f_1$  several decades lower. Note that  $K_1(1 + R_2/R_1)$  is the value of  $e_o$  at  $f = 1 \text{ Hz}$ .

Region 2;  $f_c = 100 \text{ Hz}$  to  $f_a = 673 \text{ Hz}$

$$E_{n2 \text{ rms}} = K_2 \left(1 + \frac{R_2}{R_1}\right) \sqrt{f_a - f_c} \quad (10)$$

$$= 8 \text{ nV}/\sqrt{\text{Hz}} \left(1 + \frac{10^7}{10^4}\right) \sqrt{673 - 100} \quad (10a)$$

$$= 0.21 \mu\text{V}$$

This is a region of "white" noise which leads to the form of equation (10).

Region 3;  $f_a = 673 \text{ Hz}$  to  $f_2 = 15.9 \text{ kHz}$

$$E_{n3 \text{ rms}} = K_2 \cdot K_3 \sqrt{\frac{f_2^3}{3} - \frac{f_a^3}{3}} \quad (11)$$

$$= 8 \text{ nV}/\sqrt{\text{Hz}} (1.63 \times 10^{-3}) \sqrt{\frac{(15.9 \text{ k})^3}{3} - \frac{(673)^3}{3}} \quad (11a)$$

$$= 15.1 \mu\text{V}$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance  $R_1 \parallel R_2$  and the capacitance  $(C_1 + C_2)$ . Note that  $K_3 \cdot K_2$  is the value of the  $e_o(\omega)$  function for this segment projected back to 1 Hz.

Region 4;  $f > 15.9 \text{ kHz}$

$$E_{n4 \text{ rms}} = K_2 \left(1 + \frac{C_1}{C_2}\right) \sqrt{\left[\frac{\pi}{2}\right] f_3 - f_2} \quad (12)$$

$$= 8 \text{ nV}/\sqrt{\text{Hz}} \left(1 + \frac{25}{1}\right) \sqrt{\left[\frac{\pi}{2}\right] 380 \text{ k} - 15.9 \text{ k}} \quad (12a)$$

$$= 158.5 \mu\text{V}$$

This is a region of white noise with a single order rolloff at  $f_3 = 380 \text{ kHz}$  caused by the intersection of the  $1/\beta$  curve and the open-loop gain curve. The value of 380 kHz is obtained from observing the intersection point of Figure 7. The  $\pi/2$  applied to  $f_3$  is to convert from a 3dB corner frequency to an effective noise bandwidth.

**Current Noise**

The output voltage component due to current noise is equal to:

$$E_n = i_n \times Z_2(s) \quad (13)$$

$$\text{where } Z_2(s) = R_2 \parallel X_{c_2} \quad (13a)$$

This voltage may be obtained by combining the information from figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9 below.

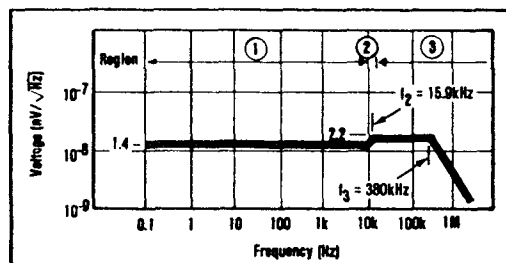
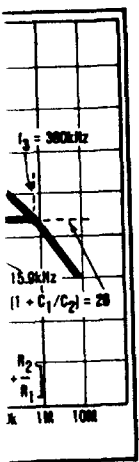


FIGURE 9. Output Voltage Due to Noise Current.

Using the same techniques that were used for the voltage noise:

Region 1; 0.1 Hz to 10 kHz



(4)

that

(5)

(5a)

(5b)

(5c)

(5d)

aches zero and

(6)

roaches infinity

(7)

(7)

$$E_{n1} = 1.4 \times 10^{-4} \sqrt{10k \cdot 0.1} \quad (14)$$

$$= 1.4 \mu V$$

Region 2; 10kHz to 15.9kHz

$$E_{n2} = 1.4 \times 10^{-12} \sqrt{\frac{(15.9k)^3}{3} - \frac{(10k)^3}{3}} \quad (14a)$$

$$= 1.4 \mu V$$

Region 3;  $f > 15.9kHz$

$$E_{n3} = 2.2 \times 10^{-8} \sqrt{\frac{\pi}{2} 380k - 15.9k} \quad (14b)$$

$$= 16.8 \mu V$$

$$E_{n_{total}} = 10^{-6} \sqrt{(1.4)^2 + (1.4)^2 + (16.8)^2} \quad (14c)$$

$$= 16.9 \mu V_{rms}$$

#### Resistor Noise

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor,  $R_2$ , must also be included. The thermal noise of the resistor is given by:

$$E_{R_{rms}} = \sqrt{4kTRB} \quad (15)$$

$k$  = Boltzmann's constant =  $1.38 \times 10^{-23}$   
Joules/°Kelvin

$T$  = Absolute temperature (degrees Kelvin)

$R$  = Resistance (ohms)

$B$  = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes

$$E_{R_{rms}} \approx 0.13 \sqrt{RB}$$

$E_{R_{rms}}$  in  $\mu V$

$R$  in  $M\Omega$

$B$  in Hz

For the circuit in Figure 4

$$R_2 = 10^7 \Omega = 10M\Omega$$

$$B = \frac{\pi}{2} (f_2) = \frac{\pi}{2} 15.9k$$

Then

$$E_{R_{rms}} = (411nV/\sqrt{Hz}) \sqrt{B}$$

$$= (411nV/\sqrt{Hz}) \sqrt{\frac{\pi}{2} 15.9kHz}$$

$$\approx 64.9 \mu V_{rms}$$

#### Total Noise

The total noise may now be computed from

$$E_{n_{total}} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{nr}^2 + E_{ni}^2} \quad (16)$$

$$= \sqrt{0.267^2 + 0.21^2 + 15.1^2 + 158.5^2 + 64.9^2 + 16.9^2} \quad (16a)$$

$$= \sqrt{0.07 + 0.04 + 228 + 25122 + 4212 + 286} \quad (16b)$$

$$= 173 \mu V_{rms}$$

#### Conclusions

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions. In this example 84% of the noise comes from  $E_{nr}$ . From Figure 8 it is seen that this is the area beyond the pole formed by  $R_2$  and  $C_2$ .

The  $E_{nr}$  contribution could be reduced several ways. The most common method is to increase  $C_2$ . This reduces  $f_2$  and the value of  $K_2(1 + C_1/C_2)$  (see Figure 8). It also reduces the signal bandwidth (see Figure 6) and the final value of  $C_2$  is normally a compromise between noise gain and necessary signal bandwidth.

It should be noted that increasing  $C_2$  will also affect  $f_1$  since  $f_1$  is determined by  $(C_1 + C_2)$  (see equation (5b)). Normally  $C_2$  is larger than  $C_1$  and  $f_2$  will change more than  $f_1$  for a given change in  $C_2$ .

The other means of reducing the noise in region 4 involves changing amplifier parameters. For example, the use of a slower amplifier would move the open-loop gain curve to the left and decrease  $f_1$ . Of course, reducing the value of  $K_2$ , the noise floor, would also reduce the noise in this region.

The second largest component is the resistor noise  $E_{nr}$  (14% of the total noise). A lower resistor value decreases resistor noise as a function of  $\sqrt{R}$ , but it also lowers the desired signal gain as a direct function of  $R$ . Thus, lowering  $R$  reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to  $R_2$  can be decreased by raising the value of  $C_2$  (lowering  $f_2$ ) but this reduces signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 1% of the total  $E_n$ . This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{characteristic} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz \quad (17)$$

$$= \frac{8nV/\sqrt{Hz}}{1.4fA/\sqrt{Hz}}$$

$$= 5.7M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the  $10M\Omega$  feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

The fourth largest component of total noise comes from  $E_{ni}$  (0.8%). Decreasing  $C_1$  will also lower the term  $K_2(1 + C_1/C_2)$ . In this case,  $f_2$  will stay fixed and  $f_1$  will move to the right (i.e., the +20dB/decade slope segment will move

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to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

**Shielding and Guarding**

The low noise, low bias current and high input impedance of the OPA101/102 are well suited to a number of precision applications. In order to fully benefit from the outstanding specifications of this unit, careful layout, shielding, and guarding are required. Careless signal wiring or printed circuit board layout can easily degrade circuit performance several orders of magnitude below the capability of the OPA101/102.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. The metal case of the OPA101/102 is connected to pin 8 and is not connected to any internal amplifier circuitry. Thus it is possible to use the case as a shield to reduce noise pickup.

Unless care is used, leakage currents across printed circuit boards can easily exceed the bias current of the OPA101/102. To avoid leakage problems, it is recommended that a Teflon IC socket be used or that at least the signal input lead of the amplifier be wired to a Teflon standoff. If this is not done and instead the OPA101/102 is to be soldered directly into a printed circuit board, utmost care must be

used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 10). The amplifier case, pin 8, should also be connected to the guard. This insures that the entire amplifier circuitry is fully surrounded by the guard potential. This minimizes the voltage placed across any leakage paths and thus reduces leakage currents. In addition, noise pickup is also reduced.

Figures 11, 12, and 13 show typical applications using the guard and case shielding.

Cleanliness is also a prime concern in low bias current circuits. It is recommended that after installation is complete the assembly be washed with a low residue solvent such as TMC Freon followed by rinsing with deionized water. The use of some form of high dielectric conformal coating such as a good two-part urathane should be considered if the assembly will be used in air environment which could deposit contaminants on the low current circuitry.

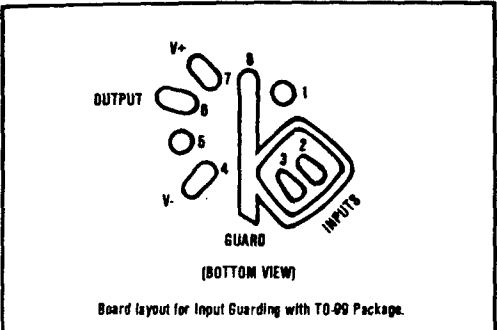


FIGURE 10. Connection of Case Guard and Input Guard.

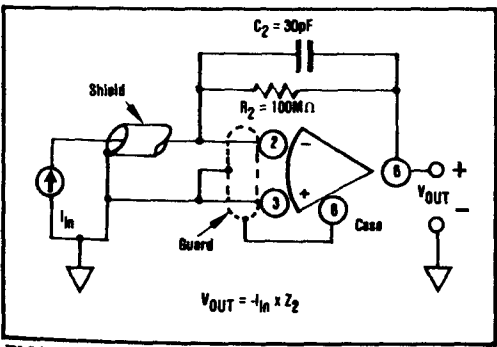


FIGURE 11. Ultra-Low Current to Voltage Converter.

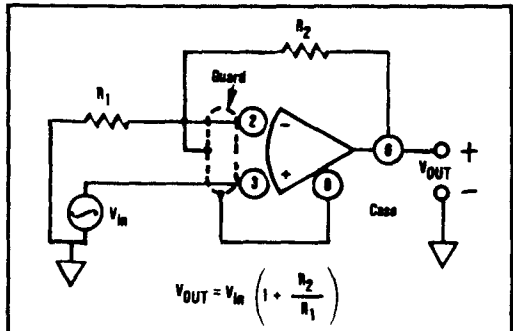


FIGURE 12. Ultra-High Input Impedance Noninverting Circuit.

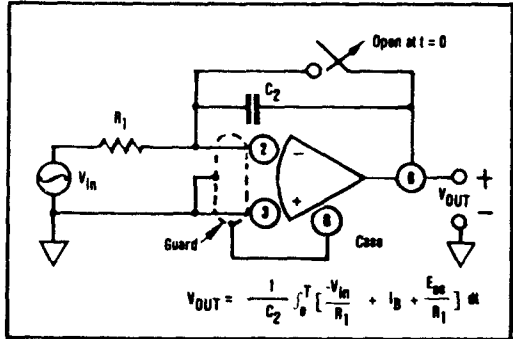


FIGURE 13. Low Drift Integrator.

**Thermal Model**

Figure 14 is the thermal model for the OPA101/102 where:  
 Tj = Junction temperature (output load)  
 Tj\* = Junction temperature (no load)  
 Tc = Case temperature  
 TA = Ambient temperature  
 θCA = Thermal resistance, case-to-ambient

(16b) together some interesting noise comes from the area beyond

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istor noise ENR value decreases also lowers the n. Thus, tio a. Output ould be as large e to R2 can be ering f2) but this

nt noise of the otal EN. This is h comparing the h the size of the define a char-

(17)

with feedback tic value, the re output noise on this and the . the amplifier have a higher e reason it does noise voltage has ) and the noise

oise comes from the term K2(1 + l f. v. ove to smel. move

$\theta_{HS}$  = Effective thermal resistance of the heat sink  
 $P_{DQ}$  = Quiescent power dissipation  
 $|+V_{CC}| I_{-QUIESCENT} + |-V_{CC}| I_{+QUIESCENT}$   
 $P_{DX}$  = Power dissipation in the output transistor  
 $= (V_{OUT} - V_{CC}) I_{OUT}$

(In a complementary output stage only one output transistor is conducting current at a time.)

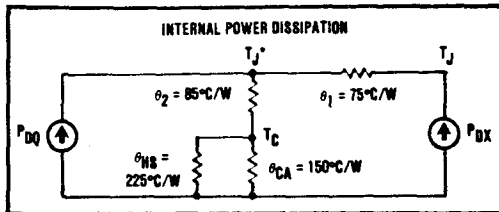


FIGURE 14. OPA101/102 Thermal Model

This model is obviously not the simple one-power source model used with most linear integrated circuits. It is, however, a more accurate model for multichip hybrid integrated circuits where the quiescent power is dissipated in the input stage and the internal power dissipation due to the load is dissipated in a somewhat physically separated output stage.

The model in Figure 14 must be used in conjunction with the OPA101/102's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem: Determine the output transistor junction temperature when the output has its maximum load resistance and is operated at the worst-case output voltage conditions. Assume  $V_{CC} = \pm 15VDC$  and  $T_A = 25^\circ C$ .

Maximum  $P_{DX}$  occurs where  $V_{OUT} = 1/2V_{CC}$ . Then

$$P_{DX \max} = \frac{(V_{CC})^2}{4R_{load}} \quad (18)$$

$$T_j = T_A + P_{DQ} [\theta_2 + (\theta_{HS} \parallel \theta_{CA})] + P_{DX} [\theta_1 + \theta_2 + (\theta_{HS} \parallel \theta_{CA})] \quad (19)$$

$$\text{where } (\theta_{HS} \parallel \theta_{CA}) = \frac{\theta_{HS}\theta_{CA}}{\theta_{HS} + \theta_{CA}} = 90^\circ C/W$$

Substituting appropriate values yields

$$\begin{aligned}
 T_j &= 25^\circ + (30V \times 8mA)[85^\circ C/W + 90^\circ C/W] \\
 &+ \frac{(15V)^2}{4 \times 1k\Omega} [75^\circ C/W + 85^\circ C/W + 90^\circ C/W] \\
 &= 25^\circ C + 42^\circ C + 14^\circ C = T_A + 56^\circ C \\
 &= 81^\circ C
 \end{aligned}$$

The conclusion is that under a worst-case output voltage condition and with a  $1k\Omega$  load the junction temperature rise is  $56^\circ C$  above ambient. Thus, under these conditions, the device could be operated in an ambient up to  $119^\circ C$  without exceeding the  $175^\circ C$  junction temperature rating.

A similar analysis for conditions of the output short-circuited to ground where

$$P_{DX \text{ SS}} = V_{CC} I_{(output \text{ limit})} \quad (20)$$

shows that the maximum junction temperature rating of  $175^\circ C$  is exceeded. Thus, the output should not be shorted to ground for sustained periods of time.

#### HEAT SINK

The heat sink used on the OPA101/102 should not be removed. It has the effect of reducing the package thermal resistance from  $150^\circ C/W$  to about  $90^\circ C$  per watt. Removing the heat sink would naturally increase the junction temperature of the amplifier which would in turn raise the input bias current. The change in thermal resistance also affects the noise performance. Removing the heat sink would increase the noise in the 1/f region.