National Semiconductor

LF147/LF347/LF347B Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description
The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (Bi-FET IITM Technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features
- Internally trimmed offset voltage: 5 mV max
- Low input bias current: 50 nA
- Low input current: 0.01 pA
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/μs
- Low supply current: 7.2 mA
- High input impedance: 10^12 Ω
- Low total harmonic distortion: 0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time: 0.01%

Simplified Schematic

Connection Diagram

Top View
Order Number: LF147D, LF347D, LF147J, LF347BJ, LF347J, LF347NM, LF347WM, LF347BN or LF347N
See NS Package Number: D14E, J14A, M14A, M14B or N14A
### Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

**LF147**

Supply Voltage
± 22V

Differential Input Voltage
± 38V

Input Voltage Range
± 18V

(Notes 1)

Output Short Circuit Duration (Note 2)
Continuous

Power Dissipation
900 mW

(Notes 3 and 9)

Tth, max
150°C

θJA
Cavity DIP (D) Package
80°C/W

Ceramic DIP (J) Package
70°C/W

Plastic DIP (N) Package
75°C/W

Surface Mount Narrow (M)
100°C/W

Surface Mount Wide (WM)
85°C/W

**LF347B/LF347**

Supply Voltage
± 18V

Differential Input Voltage
± 30V

Input Voltage Range
± 15V

(Notes 1)

Output Short Circuit Duration (Note 2)
Continuous

Power Dissipation
1000 mW

(Notes 3 and 9)

Tth, max
150°C

θJA
Cavity DIP (D) Package
80°C/W

Ceramic DIP (J) Package
70°C/W

Plastic DIP (N) Package
75°C/W

Surface Mount Narrow (M)
100°C/W

Surface Mount Wide (WM)
85°C/W

**LF147**

Operating Temperature Range
(Notes 4)

Storage Temperature Range
-65°C ≤ TA ≤ 150°C

Lead Temperature
260°C

Soldering Information
Dual-In-Line Package
Soldering (10 seconds)
260°C

Small Outline Package
Vapor Phase (60 seconds)
215°C

Infrared (15 seconds)
220°C

See AN-450 "Surface Mounting Methods and Their Effects on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

### DC Electrical Characteristics (Note 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>LF147</th>
<th>LF347B</th>
<th>LF347</th>
<th>Units</th>
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<td>Min</td>
<td>Typ</td>
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<tr>
<td>VOS</td>
<td>Input Offset Voltage</td>
<td>RθS = 10 kΩ, TA = 25°C Over Temperature</td>
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<td>ΔVos/ΔT</td>
<td>Average TC of Input Offset Voltage</td>
<td>RθS = 10 kΩ</td>
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<td>IOS</td>
<td>Input Offset Current</td>
<td>Tj = 25°C, (Notes 5, 8) Over Temperature</td>
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<td>100</td>
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<td>IB</td>
<td>Input Bias Current</td>
<td>Tj = 25°C, (Notes 5, 8) Over Temperature</td>
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<td>RIN</td>
<td>Input Resistance</td>
<td>Tj = 25°C</td>
<td>1012</td>
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<td>AVOL</td>
<td>Large Signal Voltage Gain</td>
<td>Vθ = ±15V, TA = 25°C Over Temperature</td>
<td>50</td>
<td>100</td>
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<td>100</td>
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<td>VO</td>
<td>Output Voltage Swing</td>
<td>Vθ = ±15V, RA = 10 kΩ</td>
<td>± 12</td>
<td>± 13.5</td>
<td>± 12</td>
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<td></td>
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<td>± 12</td>
<td>± 13.5</td>
<td>± 12</td>
<td>± 13.5</td>
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<tr>
<td>VCM</td>
<td>Input Common-Mode Voltage Range</td>
<td>Vθ = ±15V</td>
<td>± 11</td>
<td>+ 15</td>
<td>± 11</td>
<td>+ 15</td>
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<tr>
<td></td>
<td></td>
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<td>± 12</td>
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<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>RθS ≤ 10 kΩ</td>
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<td>PSRR</td>
<td>Supply Voltage Rejection Ratio</td>
<td>(Note 7)</td>
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<td>IS</td>
<td>Supply Current</td>
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### AC Electrical Characteristics (Note 5)

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<th>LF347/B</th>
<th>LF347</th>
<th>Units</th>
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<tr>
<td></td>
<td>Amplifier to Amplifier Coupling</td>
<td>$T_A = 25°C$, $f = 1$ Hz – 20 kHz (Input Referred)</td>
<td>-120</td>
<td>-120</td>
<td>-120</td>
<td>dB</td>
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<td>SR</td>
<td>$V_R = \pm 15V, T_A = 25°C$</td>
<td>8</td>
<td>13</td>
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<td>13</td>
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<td></td>
<td>GBW</td>
<td>$V_R = \pm 15V, T_A = 25°C$</td>
<td>2.2</td>
<td>4</td>
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<tr>
<td>$I_n$</td>
<td>Equivalent Input Noise Voltage</td>
<td>$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000$ Hz</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>nV/$\sqrt{Hz}$</td>
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<tr>
<td>$I_v$</td>
<td>Equivalent Input Noise Current</td>
<td>$T_J = 25°C$, $I = 1000$ Hz</td>
<td>0.01</td>
<td>0.01</td>
<td>0.01</td>
<td>pA/$\sqrt{Hz}$</td>
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</tbody>
</table>

**Note 1:** Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

**Note 2:** Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

**Note 3:** For operating at elevated temperatures, these devices must be derated based on a thermal resistance of $\theta_{JA}$.

**Note 4:** The LF147 is available in the military temperature range $-55°C \leq T_A \leq 125°C$, while the LF347/B and the LF347 are available in the commercial temperature range $0°C \leq T_A \leq 70°C$. Junction temperature can rise to $T_J = 150°C$.

**Note 5:** Unless otherwise specified the specifications apply over the full temperature range and for $V_R = \pm 10V$ for the LF147 and for $V_R = \pm 15V$ for the LF347/B.

**Note 6:** Input bias currents are junction leakage currents which approximately double for every $10°C$ increase in the junction temperature, $T_J$. Due to wide production lot time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation. $P_J = T_J - \theta_{JA} P_D$ where $\theta_{JA}$ is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias currents is to be kept to a minimum.

**Note 7:** Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_R = \pm 8V$ to $\pm 15V$ for the LF347/B and from $V_R = \pm 20V$ to $\pm 5V$ for the LF147.

**Note 8:** Refer to RETS147X for LF147D and LF147 military specifications.

**Note 9:** Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.
Typical Performance Characteristics

- **Input Bias Current**
  - 
  
- **Supply Current**
  - 
  
- **Positive Common-Mode Input Voltage Limit**
  - 
  
- **Negative Common-Mode Input Voltage Limit**
  - 
  
- **Positive Current Limit**
  - 
  
- **Negative Current Limit**
  - 
  
- **Output Voltage Swing**
  - 
  
- **Gain Bandwidth**
  - 
  
- **Bode Plot**
  - 
  
- **Slew Rate**
  - 

TLH/5567-2
Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (Bi-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier...
Application Hints (Continued)

Output to a high state. In neither case does a latch occur
since raising the input back within the common-mode range
again puts the input stage and thus the amplifier in a normal
operating mode.

Exceeding the positive common-mode limit on a single input
will not change the phase of the output; however, if both
inputs exceed the limit, the output of the amplifier will be
forced to a high state.

The amplifiers will operate with a common-mode input volt-
age equal to the positive supply; however, the gain band-
width and slew rate may be decreased in this condition.
When the negative common-mode voltage swings to within
3V of the negative supply, an increase in input offset voltage
may occur.

Each amplifier is individually biased by a zener reference
which allows normal circuit operation on ±4.5V power sup-
plies. Supply voltages less than these may result in lower
gain bandwidth and slew rate.

The LF147 will drive a 2 kΩ load resistance to ±10V over
the full temperature range. If the amplifier is forced to drive
heavier load currents, however, an increase in input offset
voltage may occur on the negative voltage swing and finally
reach an active current limit on both positive and negative
swings.

Precautions should be taken to ensure that the power sup-
ply for the integrated circuit never becomes reversed in po-
larly or that the unit is not inadvertently installed back-
wards in a socket as an unlimited current surge through the
resulting forward diode within the IC could cause fusing of
the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET
input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead
wires, component placement and supply decoupling in or-
der to ensure stability. For example, resistors from the out-
pot to an input should be placed with the body close to the
input to minimize "pick-up" and maximize the frequency of
the feedback pole by minimizing the capacitance from the
input to ground.

A feedback pole is created when the feedback around any
amplifier is resistive. The parallel resistance and capacit-
ance from the input of the device (usually the inverting in-
put) to AC ground set the frequency of the pole. In many
instances the frequency of this pole is much greater than
the expected 3 dB frequency of the closed loop gain and
consequently there is negligible effect on stability margin.
However, if the feedback pole is less than approximately 6
times the expected 3 dB frequency a lead capacitor should
be placed from the output to the input of the op amp. The
value of the added capacitor should be such that the RC
time constant of this capacitor and the resistance it parallels
is greater than or equal to the original feedback pole time
constant.

Detailed Schematic
Typical Applications

Digitally Selectable Precision Attenuator

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>V₀</th>
<th>Attenuation</th>
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<td>0</td>
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<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>-1 dB</td>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>-2</td>
<td>-2 dB</td>
</tr>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-7</td>
<td>-7 dB</td>
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</table>

All resistors 1% tolerance

- Accuracy of better than 0.4% with standard ±% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment

* \( V_{OUT} \) starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

\[
V_{OUT} = \frac{1}{RC} \int (V_{IN} - V_{TH}) dt
\]

* Output starts when \( V_{IN} > V_{TH} \)
* Switch S1 permits stopping and holding any output value
* Switch S2 resets system to zero
Typical Applications (Continued)

Universal State Variable Filter

For circuit shown:
- 3 kHz, notch = 8.5 kHz
- Q = 3.4
- Passband gain:
  - Highpass = 0.1
  - Bandpass = 1
  - Lowpass = 1
  - Notch = 10

  + $f_p \times Q \leq 200$ kHz
  + 10V peak sinusoidal output swing without slew limiting to 200 kHz
  + See LM148 data sheet for design equations