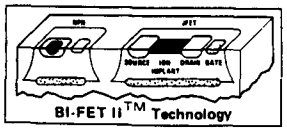
National Semiconductor



LF13508 8-Channel Analog Multiplexer
LF13509 4-Channel Differential Analog Multiplexer

General Description

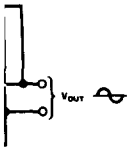
The LF13508 is an 8-channel analog multiplexer which connects the output to 1 of the 8 analog inputs depending on the state of a 3-bit binary address. An enable control allows disconnecting the output, thereby providing a package select function.

This device is fabricated with National's BI-FET technology which provides ion-implanted JFETs for the analog switch on the same chip as the bipolar decode and switch drive circuitry. This technology makes possible low constant "ON" resistance with analog input voltage variations. This device does not suffer from latch-up problems or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action.

The LF13509 is a 4-channel differential analog multiplexer. A 2-bit binary address will connect a pair of independent analog inputs to one of any 4 pairs of independent analog outputs. The device has all the features of the LF13508 series and should be used whenever differential analog inputs are required.

Features

- JFET switches rather than CMOS
- No static discharge blow-out problem
- No SCR latch-up problems
- Analog signal range 11V, −15V
- Constant "ON" resistance for analog signals between −11V and 11V
- "ON" resistance 380 Ω typ
- Digital inputs compatible with TTL and CMOS
- Output enable control
- Break-before-make action: $t_{OFF} = 0.2\ \mu s$; $t_{ON} = 2\ \mu s$ typ
- Lower leakage devices available



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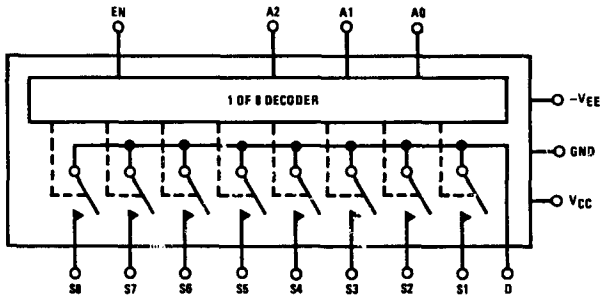
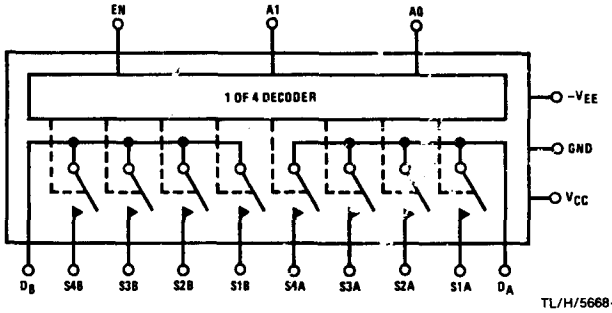
Functional Diagrams and Truth Tables

LF13508



EN	A2	A1	A0	SWITCH ON
H	L	L	L	S1
H	L	L	H	S2
H	L	H	L	S3
H	L	H	H	S4
H	H	L	L	S5
H	H	L	H	S6
H	H	H	L	S7
H	H	H	H	S8
L	X	X	X	NONE

LF13509



EN	A1	A0	SWITCH PAIR ON
L	X	X	None
H	L	L	S1
H	L	H	S2
H	H	L	S3
H	H	H	S4

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply − Negative Supply ($V_{CC}-V_{EE}$)	36V
Positive Analog Input Voltage (Note 1)	V_{CC}
Negative Analog Input Voltage (Note 1)	$-V_{EE}$
Positive Digital Input Voltage	V_{CC}
Negative Digital Input Voltage	−5V
Analog Switch Current	$\|I_S\| < 10$ mA

Power Dissipation (P_D at 25°C) (Notes 2 & 7)		
Molded DIP (N)	P_D	500 mW
Cavity DIP (D)	P_D	900 mW
Maximum Junction Temperature (T_{jMAX})		100°C
Operating Temperature Range		$0°C \le T_A \le +70°C$
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		300°C

Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions		LF13508 LF13509 Min	Typ	Max	Units
R_{ON}	"ON" Resistance	$V_{OUT}=0V$, $I_S=100\ \mu A$	$T_A=25°C$		380	650	Ω
					500	850	Ω
ΔR_{ON}	ΔR_{ON} with Analog Voltage Swing	$-10V \le V_{OUT} \le +10V$, $I_S=100\ \mu A$	$T_A=25°C$		0.01	1	%
R_{ON} Match	R_{ON} Match Between Switches	$V_{OUT}=0V$, $I_S=100\ \mu A$	$T_A=25°C$		20	150	Ω
$I_{S(OFF)}$	Source Current in "OFF" Condition	Switch "OFF", $V_S=11$, $V_D=-11$, (Note 4)	$T_A=25°C$			5	nA
					0.09	50	nA
$I_{D(OFF)}$	Drain Current in "OFF" Condition	Switch "OFF", $V_S=11$, $V_D=-11$, (Note 4)	$T_A=25°C$			20	nA
					0.6	500	nA
$I_{D(ON)}$	Leakage Current in "ON" Condition	Switch "ON" $V_D=11V$, (Note 4)	$T_A=25°C$			20	nA
					1	500	nA
V_{INH}	Digital "1" Input Voltage			2.0			V
V_{INL}	Digital "0" Input Voltage					0.7	V
I_{INL}	Digital "0" Input Current	$V_{IN}=0.7V$	$T_A=25°C$		1.5	30	μA
						40	μA
$I_{INL(EN)}$	Digital "0" Enable Current	$V_{EN}=0.7V$	$T_A=25°C$		1.2	30	μA
						40	μA
t_{TRAN}	Switching Time of Multiplexer	*(Figure 1)*, (Note 5)	$T_A=25°C$		1.8		μs
t_{OPEN}	Break-Before-Make	*(Figure 3)*	$T_A=25°C$		1.6		μs
$t_{ON(EN)}$	Enable Delay "ON"	*(Figure 2)*	$T_A=25°C$		1.6		μs
$t_{OFF(EN)}$	Enable Delay "OFF"	*(Figure 2)*	$T_A=25°C$		0.2		μs
$I_{SO(OFF)}$	"OFF" Isolation	(Note 6)	$T_A=25°C$		−66		dB
CT	Crosstalk	LF13509 Series, (Note 6)	$T_A=25°C$		−66		dB
$C_{S(OFF)}$	Source Capacitance ("OFF")	Switch "OFF", $V_{OUT}=0V$, $V_S=0V$	$T_A=25°C$		2.2		pF
$C_{D(OFF)}$	Drain Capacitance ("OFF")	Switch "OFF", $V_{OUT}=0V$, $V_S=0V$	$T_A=25°C$		11.4		pF
I_{CC}	Positive Supply Current	All Digital Inputs Grounded	$T_A=25°C$		7.4	12	mA
					7.9	15	mA
I_{EE}	Negative Supply Current	All Digital Inputs Grounded	$T_A=25°C$		2.7	5	mA
					2.8	6	mA

Note 1: *If the analog input voltage exceeds this limit, the input current should be limited to less than 10 mA.*

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{jMAX}-T_A)/\theta_{jA}$ or the 25°C P_{DMAX}, whichever is less.

Note 3: These specifications apply for $V_S=\pm15V$ and over the absolute maximum operating temperature range ($T_L \le T_A \le T_H$) unless otherwise noted.

Note 4: Conditions applied to leakage tests insure worse case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".

Note 5: Lots are sample tested to this parameter. The measurement conditions of *Figure 1* insure worse case transition time.

Note 6: "OFF" isolation is measured with all switches "OFF" and driving a source. Crosstalk is measured with a pair of switches "ON", driving channel A and measuring channel B. $R_L=200$, $C_L=7$ pF, $V_S=3$ Vrms, $f=500$ kHz.

Note 7: Thermal Resistance θ_{jA} (Junction to Ambient)

Molded DIP (N)	150°C/W
Cavity DIP (D)	100°C/W

	500 mW
	900 mW
$(T_j$	100°C
	$0°C \leq T_A \leq +70°C$
	$-65°C$ to $+150°C$
0 sec.)	300°C

LF13508 LF13509			Units
Min	Typ	Max	
	380	650	Ω
	500	850	Ω
	0.01	1	%
	20	150	Ω
		5	nA
	0.09	50	nA
		20	nA
	0.6	500	nA
		20	nA
	1	500	nA
2.0			V
		0.7	V
	1.5	30	μA
		40	μA
	1.2	30	μA
		40	μA
	1.8		μs
	1.6		μs
	1.6		μs
	0.2		μs
	−66		dB
	−66		dB
	2.2		pF
	11.4		pF
	7.4	12	mA
	7.9	15	mA
	2.7	5	mA
	2.8	6	mA

MAX, θ_{jA}, and the ambient temperature, is less.

$\leq T_H$) unless otherwise noted.

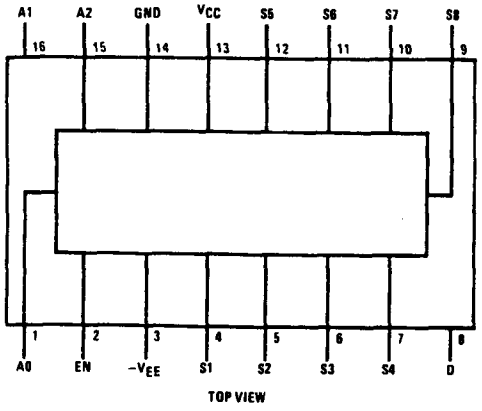
an "OFF" channel to turn "ON".

ime.

switches "ON", driving channel A and

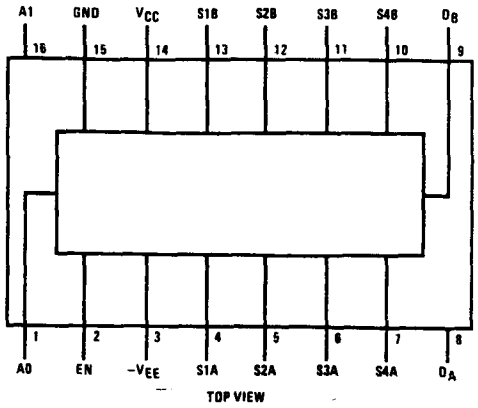
Connection Diagrams

LF13508
Dual-In-Line Package



Order Number LF13508D
See NS Package Number D16C
Order Number LF13508N
See NS Package Number N16A

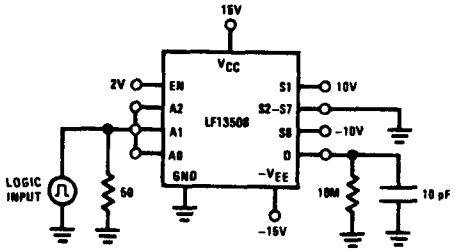
LF13509
Dual-In-Line Package

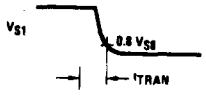


TL/H/5668–2

Order Number LF13509D
See NS Package Number D16C
Order Number LF13509N
See NS Package Number N16A

AC Test Circuits and Switching Time Waveforms





TL/H/5668–3

FIGURE 1. Transition Time

AC Test Circuit and Switching Time Waveforms (Continued)

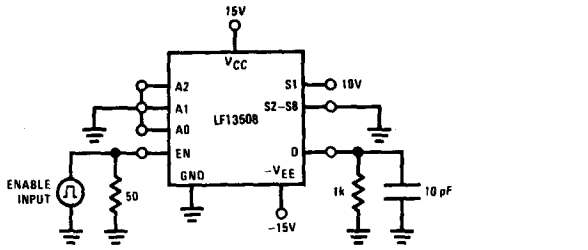
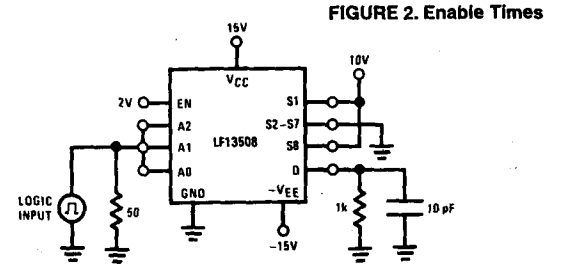


FIGURE 2. Enable Times

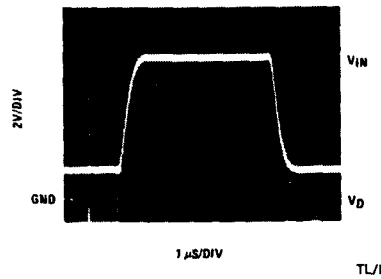


TL/H/5668–4

FIGURE 3. Break-Before-Make

Transition Times and Transients

V_A = 10V



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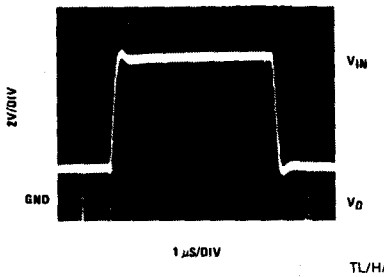
V_A = 5V



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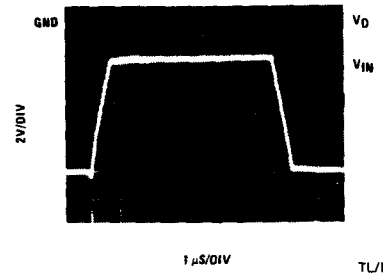
V_A = 0V



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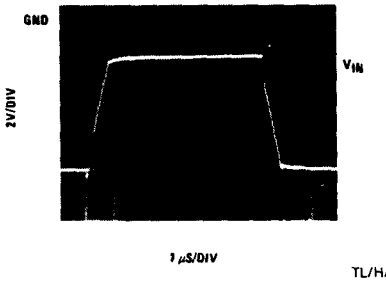
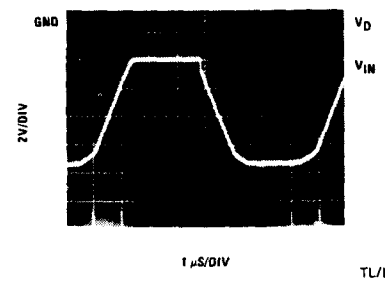
V_A = −5V



TL/H/5668–8

V_A = −10V



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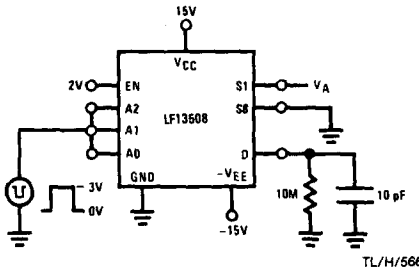
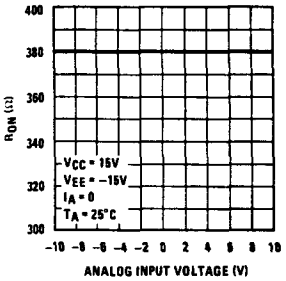
Test Circuit



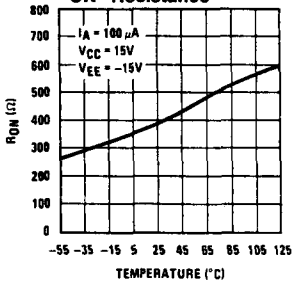
TL/H/5668–10

Typical Performance Characteristics

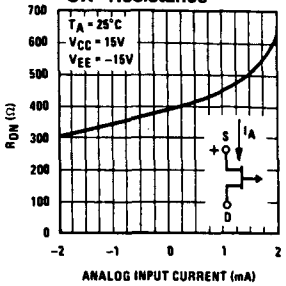
"ON" Resistance



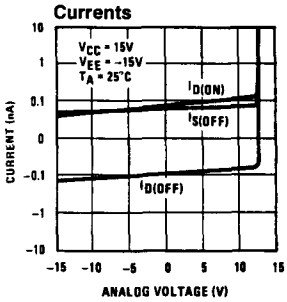
"ON" Resistance



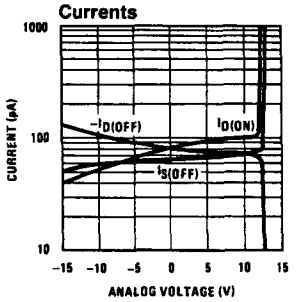
"ON" Resistance



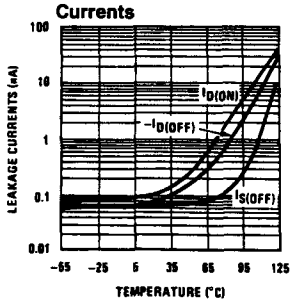
Switch Leakage Currents



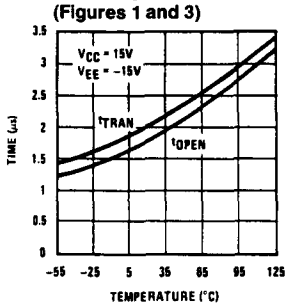
Switch Leakage Currents



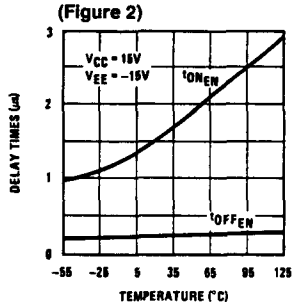
Switch Leakage Currents



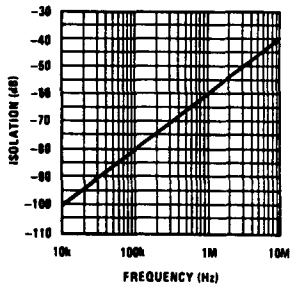
Switching Times (Figures 1 and 3)



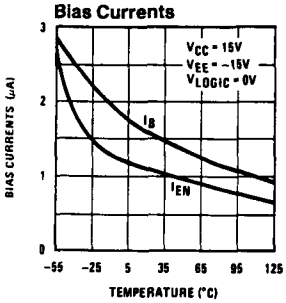
Enable Delay Times (Figure 2)



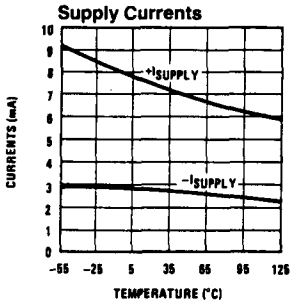
"OFF" Isolation and Crosstalk



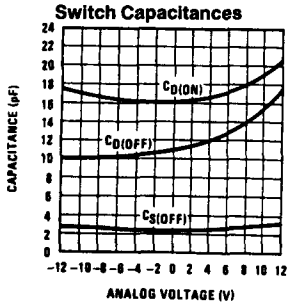
Bias Currents



Supply Currents



Switch Capacitances



TL/H/5668-11

Application Hints

The LF11508 series is an 8-channel analog multiplexer which allows the connection of a single load to 1 of 8 different analog inputs. These multiplexers incorporate JFETs in a switch configuration which insures a constant "ON" resistance over the analog voltage range of the device. Four TTL compatible inputs are provided; a 3-bit binary decode to select a particular channel and an enable input used as a package select. The switches operate with a break-before-make action preventing the temporary connection of 2 analog inputs during switching. Because these multiplexers are fabricated with the BI-FET process rather than CMOS, they do not require special handling.

The LF11509 series is a 4-channel differential multiplexer which allows two loads to be connected to 1 of 4 different pairs of analog inputs. The LF11509 series also has all the features of the LF11508.

ANALOG VOLTAGE AND CURRENT

The "ON" resistance, R_{ON}, of the analog switches is constant over a wide input range from positive (V_{CC}) supply to negative ($-V_{EE}$) supply.

The analog input should not exceed either positive or negative supply without limiting the current to less than 10 mA; otherwise the multiplexer may get damaged. For proper operation, however, the positive analog voltage should be kept equal to or less than $V_{CC} - 4V$ as this will increase the switch leakage in both "ON" and "OFF" state and it may also cause a false turn "ON" of a normally "OFF" switch. This limit applies over the full temperature range.

The maximum allowable switch "ON" voltage (the drop across the switch in the "ON" condition) is $\pm 0.4V$ over temperature. If this number is to exceed the input current should be limited to 10 mA.

The "ON" resistance of the multiplexing switches varies slightly with analog current because they are JFETs running at 0V gate to source. The JFET characteristics shown in *Figure 4* indicates how R_{ON} tends to vary with current. A lower R_{ON} is possible when the source voltage is negative with respect to the drain voltage because the JFET becomes enhanced. Caution should be used when operating in this mode as this may forward-bias an internal transistor and cause high currents to flow in the switches. Thus, the drain voltage should never be greater than 0.4V positive with respect to the source voltage without limiting the drain current to less than 10 mA.

LEAKAGE CURRENTS

Leakage currents will remain within the specified value as long as the drain and source remain within the specified analog voltage range. As the switch terminals exceed the positive analog voltage range "ON" and "OFF" leakage currents increase. The "ON" leakage increases due to an internal clamp required by the switch structure. The "OFF" leakage increases because the gate to source reverse bias has been decreased to the point where the switch becomes active. Leakage currents vary slightly with analog voltage and will approximately double for every 10°C rise in temperature.

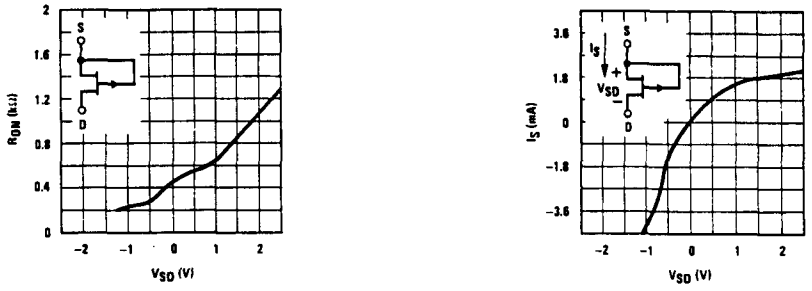
SWITCHING TIMES AND TRANSIENTS

These multiplexers operate with a break-before-make switch action. The turn off time is much faster than the turn on time to guarantee this feature over the full range of analog input voltage and temperature. Switching transients are introduced when a switch is turned "OFF". The amplitude of these transients may be reduced by increasing the load capacitance or decreasing the load resistance. The actual charge transfer in the transient may be reduced by operating on reduced power supplies. Examples of switching times and transients are shown in the typical characteristic curves. The enable function switching times are specified separately from switch-to-switch transition times and may be thought of as package-to-package transition times.

LOGIC INPUTS AND ENABLE INPUT

Switch selection in the LF11508 series is accomplished by using a 3-bit binary decode while the LF11509 series uses a 2-bit decode. These binary logic inputs are compatible with both TTL and CMOS logic voltage levels. The maximum positive voltage applied to these inputs may exceed V_{CC} but should not exceed $-V_{EE}+36V$. The maximum negative voltage should not be less than 4V below ground as this will cause an internal device to zener and all the switches will turn "ON".

As shown in the schematic diagram, the logic low bias current will flow until the PNP input is raised above the 3 diode reference ($\approx 2.1V$). Above this voltage the input device becomes reverse biased and the input current drops to the leakage of the reverse biased junction ($<0.1\ \mu A$).



TL/H/5668–12

FIGURE 4. JFET Characteristics

Typical Applications

DATA ACQUISITION SYSTEM

A SIMPLIFIED SYSTEM DISCUSSION

Analog multiplexers (MUX) are usually used for multi-channel Data Acquisition Units (DAU). *Figure 5* shows a system in which 8 different analog inputs are sampled and converted into digital words for further processing. The sample and hold circuit is optional, depending on input speed requirements and on A/D converter speed.

Parameters characterizing the system are:

System Channels: The number of multiplexer channels.

Accuracy: The conversion accuracy of each individual sample with the system operating at the throughput rate.

Speed or Throughput Rate: Number of samples/second/channel the system can handle.

For a discussion on system structure, addressing mode and processor interfacing, see application note AN-159.

A. ACCURACY CONSIDERATIONS

1. Multiplexer's Influence on System Accuracy *(Figure 6)*.

   a. The error, (E), caused by the finite "ON" resistance, R_{ON}, of the multiplexing switches is given by:

$$E(\%) = \frac{100}{1 + R_{IN}/(R_{ON} + R_S + \Delta R_{ON})} \text{ where:}$$

   R_{IN} = following stage input impedance

   ΔR_{ON} = "ON" resistance modulation which is negligible for JFET switches like the LF11508

   Example: Let R_{ON} = 450 Ω, ΔR_{ON} = 0, R_S = 0, T_A = 25°C and allowable E = 0.01% which is equivalent to 1/2 LSB in a 12-bit system:

$$R_{IN}\Big|_{min} = \frac{R_{ON}(100 - E)}{E} = 4.5\ M\Omega$$

   Note that if temperature effects are included, some gain (or full scale) drift will occur; but effects on linearity are small.

   b. Multiplexer settling time (t_s):

   $t_{s(ON)}$: is the time required for the MUX output to settle within a predetermined accuracy, as shown in Table I.

   C_S *(Figure 6)*: MUX output capacitance + following stage input capacitance + any stray capacitance at this node.

TABLE I.

ERROR %	BITS	t_s(ON) TO 1/2 LSB
0.2	8	6.2t
0.05	10	7.6t
0.01	12	9t
0.0008	16	11.8t

$$t = C_S (R_{ON} + R_S) \parallel R_{IN}$$

   $t_{s(OFF)}$: is the time it takes to discharge C_S within a tolerable error. The "OFF" settling time should be taken into account for bipolar inputs where its effects will appear as a worse case of doubling of the $t_{s(ON)}$.

2. Sample and Hold Influence on System Accuracy

   The sample and hold, if used, also introduces errors into the system accuracy due to:
   - Offset voltage of sample and hold
   - Droop rate in the Hold mode
   - T_A: Aperture time or time delay between the time of a digital Hold command and the actual Hold occurance
   - Taq: Acquisition time or time it takes to acquire an analog input and settle within a predetermined error band
   - Hold step: Error created during the Sample to Hold mode caused by an undesirable charge injected into the Hold capacitor C_h.

   For more details on sample and hold errors, see the LF198/LF298/LF398 data sheet.

3. A/D Converter Influence on System Accuracy

   The "accuracy" of the A/D converter is the best possible system accuracy. In most data acquisition systems, the A/D converter is the most expensive single component, so its error will often dominate system error. Care should be taken that MUX, S/H and input source errors do not exceed system error requirements when *added* to A/D errors. For instance, if an 8-bit accuracy system is desired and an 8-bit A/D converter is used, the accuracy of the MUX and S/H should be far better than 8 bits.

For details on A/D converter specifications, see AN-156.

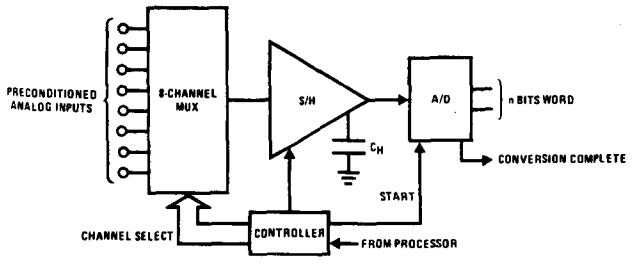


FIGURE 5. Random-Addressed, Multiplexed DAU

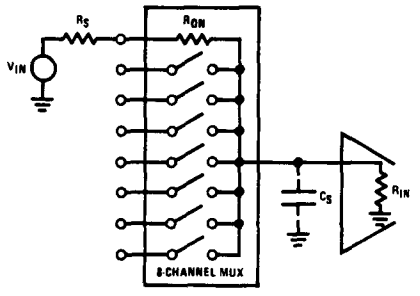


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FIGURE 6. 8-Channel MUX

Typical Applications (Continued)

B. SPEED CONSIDERATIONS

In the system of *Figure 5* with the S/H omitted, if n-bit accuracy is desired, the change of the analog input voltage should be less than ±1/2 LSB over the A/D conversion time T_C. In other words, the analog input slew rate, (rate of change of input voltage), will cause a slew-induced error and its magnitude, with respect to the total system error, will depend on the particular application.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{\pm 1/2\ LSB}{T_C} = \frac{V_{FS}}{2^n \times T_C}$$

where V_{FS} is the full scale voltage of the A/D. Note that slew induced errors are not affected by the MUX switch time since we can let the unit settle before starting conversion.

Example: Let $T_C = 40\ \mu s$ (MM4357), $V_{FS} = 10V$ and $n = 8$.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{1mV}{\mu s}$$

which is a very small number. A 10 Vp-p sine wave of a frequency greater than 32 Hz will have higher slew rate than this. The maximum throughput rate of the above 8-channel system would be calculated using both the A/D conversion time and the sum of MUX switch "ON" time and settling time, i.e.:

$$\text{Th. R}\Big|_{max} = \frac{1}{8(T_C + T_{MUX})} = 3k\ \text{samples/sec/channel}$$

$$T_{MUX} = T_{ON} + T_{S(ON)}$$

Also notice that Nyquist sampling criteria would allow each channel to have a signal bandwidth of 1.5 kHz max, while the slew limit dictates a maximum frequency of 32 Hz. If the input signal has a peak-to-peak voltage less than 10V, the allowable maximum input frequency can be calculated by:

$$f_{MAX} = \frac{(\text{Slew Rate})max}{\pi\ Vp\text{-}p}$$

On the other hand, if the input voltage is not band-limited a low pass filter with an attenuation of 30 dB or better at 1.5 kHz, should be connected in front of the MUX.

1. Improving System Speed with a Sample and Hold

   The system speed can be improved by using the S/H shown in *Figure 5*. This allows a much greater rate of change of V_{IN}.

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{V_{FS}}{2^n \times T_A}$$

where T_A is the aperture time of the S/H. This represents an input slew rate improvement by a factor: T_C/T_A. Here again, the slew rate error is not affected by the acquisition time of the Sample and Hold since conversion will start after the S/H has settled. *An important thing to notice is that the sample and hold errors will add to the total system error budget; therefore, the inequality of the $\Delta V_{IN}/\Delta t$ expression should become more stringent.*

Example: $T_C = 40\ \mu s$, $T_A = 0.5\ \mu s$, $n = 8$: $T_C/T_A = 80$

So the use of a S/H allows a speed improvement by nearly two orders of magnitude.

The maximum throughput rate can be calculated by:

$$\text{Th. R}\Big|_{max} = \frac{1}{8(T_A + Taq + T_C)}$$

Notice that T_{MUX} does not affect the $\Delta V_{IN}/\Delta t$ expression *nor the throughput rate* of the system since it may be switched and settled while the Sample and Hold is in the Hold mode. This is true, provided that: $T_{MUX} < T_A + T_C$.

C. SYSTEM EXAMPLE *(Figure 7)*

The LF398 S/H with a 1000 pF hold capacitor, has an acquisition time of 4 μs to 0.1% (1/4 LSB error for 8 bits) and an aperture time of less than 200 μs. On the other hand, after the hold command, the output will settle to ±0.05 mV in 1 μs. This, together with the acquisition time, introduces approximately a ±1/4 LSB error. Allowing another 1/4 LSB error for hold step and gain non-linearity, the maximum slew error ($\Delta V_{IN}/\Delta t$) should not exceed 1/4 LSB or:

$$\frac{\Delta V_{IN}}{\Delta t} \leq \frac{1}{4} \times \frac{1}{256} \times \frac{1}{T_A} \approx 5mV/\mu s$$

(which is the maximum slew rate of a 5 V peak sine wave. Also notice that, due to the above input slew restrictions, the analog delay caused by the finite BW of the S/H and the digital delay caused by the response time of the controller will be negligible. The maximum throughput rate of the system is:

$$\text{Th. R}\Big|_{max} = \frac{1}{8(5 + 40)10^{-6}} = 2800\ \text{samples/sec/ch.}$$

If the system speed requirements are relaxed, but the A/D converter is still too slow, then an inexpensive S/H can be built by using just a capacitor and a low cost FET input op amp as shown in *Figure 8*.

Typical Applications (Continued)

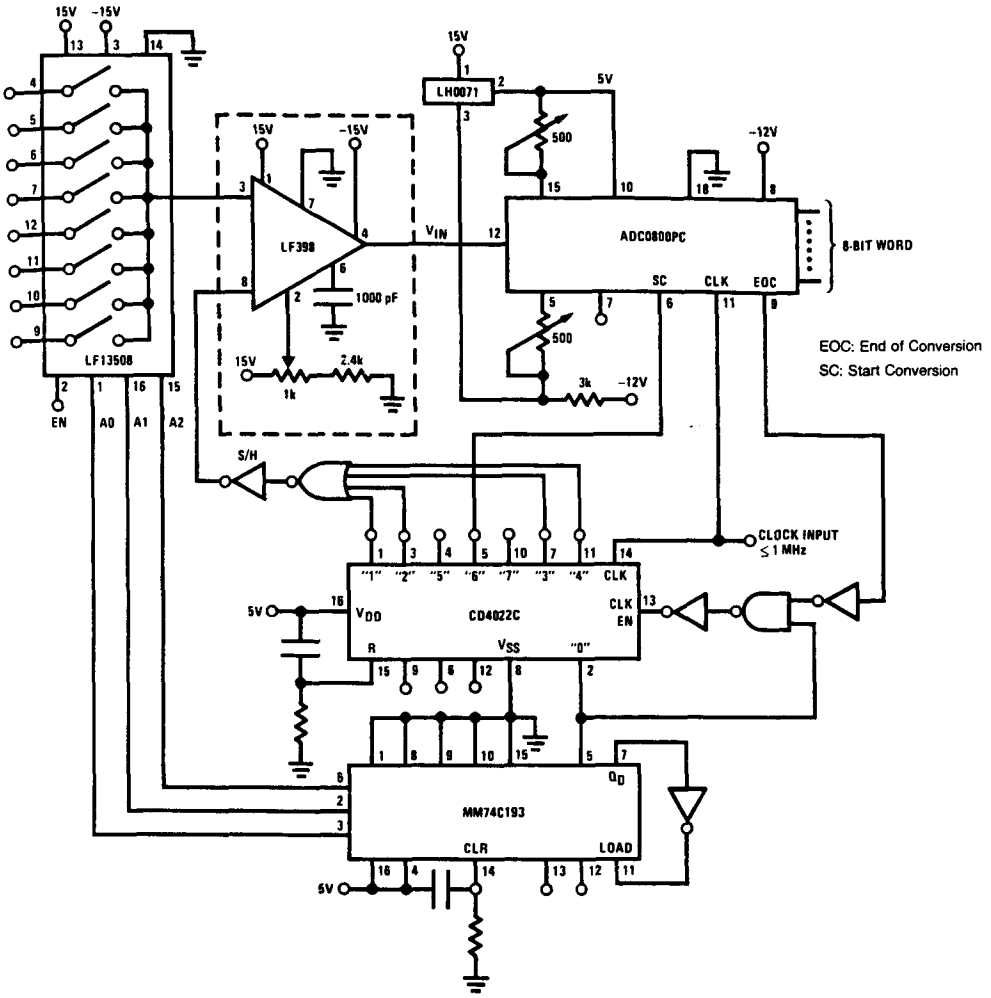

FIGURE 7a. Sequentially Multiplexed DAU with Sample and Hold

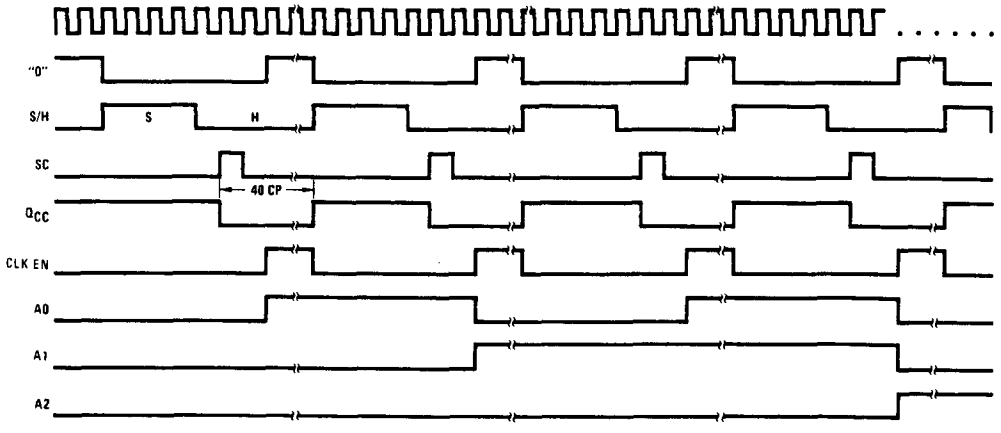

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FIGURE 7b. Timing Diagram

Typical Applications (Continued)

D. DOUBLING THE SYSTEM CHANNEL CAPABILITY

This is done in two different ways. First, we can use second level multiplexing with speed benefits, as shown in *Figure 9.* A fast 2-channel multiplexer, made by the dual analog switch AM182, accepts the outputs of each 8-channel MUX, LF13508, and then feeds them sequentially into an 8-bit successive approximation A/D converter. With this technique, the throughput rate of the system can again be made independent of the LF13508 speed. Looking at the timing diagram, when the A/D converter converts the analog value of an upper multiplexer channel, we switch channels in the lower multiplexer for the next conversion. This can be done provided that:

$$T_{MUX} \leq T_C + 1\,CP$$

The LF356 connected as unity gain buffers are used because of the low input impedance of the A/D; they are connected between multiplexers for speed optimization. With a maximum clock frequency of 4.5 MHz:

$$\text{Th. R} = \frac{10^6}{16 \times 2} = 31.25\text{k samples/sec/channel}$$

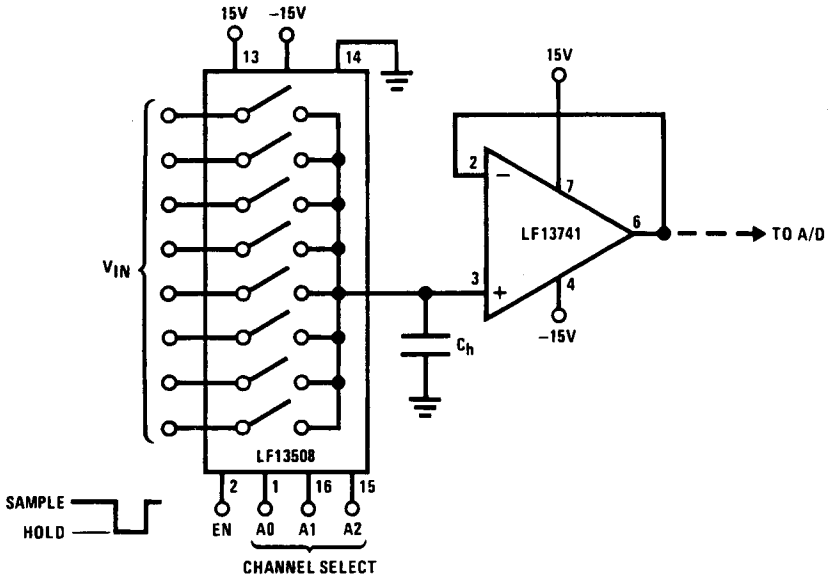
and

$$\left.\frac{\Delta V_{IN}}{\Delta t}\right|_{max} < \frac{10}{256} \times \frac{1}{2\mu s} = 19.5\ \text{mV}/\mu\text{s for } 10V_{FS}$$

An alternate way to increase the system channel is shown in *Figure 10,* where the enable pins are used to disable one MUX while the other is sampling. With this method, many 8-channel multiplexers can be connected, but the parasitic capacitance at the common output node will keep increasing and will eventually degrade the settling time, $t_{s(ON)}$. Also, the MUX speed will now affect the system throughput. If, for instance, this method was used instead of second level multiplexing, the system of *Figure 9* will lose half of its speed. If, however, speed is not the prime system requirement, the approach of *Figure 10* is more cost effective.

E. DIFFERENTIAL INPUT SYSTEMS

Systems operating in industrial environments may require an instrumentation amplifier to separate the desired analog signal from any common-mode signal present. The LF11509 was designed to provide 4 pairs of differential input signals to the input of an instrumentation amplifier for further process. A 4-channel preconditioning circuit is shown in *Figure 11* and a complete system is shown in *Figure 12.*



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- The acquisition time, T_A, of the Sample and Hold depends upon: R_{ON}, I_{DSS} of switches, Z_{OUT} of switches
- $I_{DSS} \geq 1.5$ mA, $Z_{OUT} = 40$ kΩ
- $V_{IN} = 10V$, $C_h = 1000$ pF, $T_A = 20$ μs to 0.1%
- Error created by charge injection during Hold mode: $\Delta V_E \geq 10$ pF $(14.5V - V_{IN})/C_h$

FIGURE 8. Inexpensive Sample and Hold

Typical Applications (Continued)

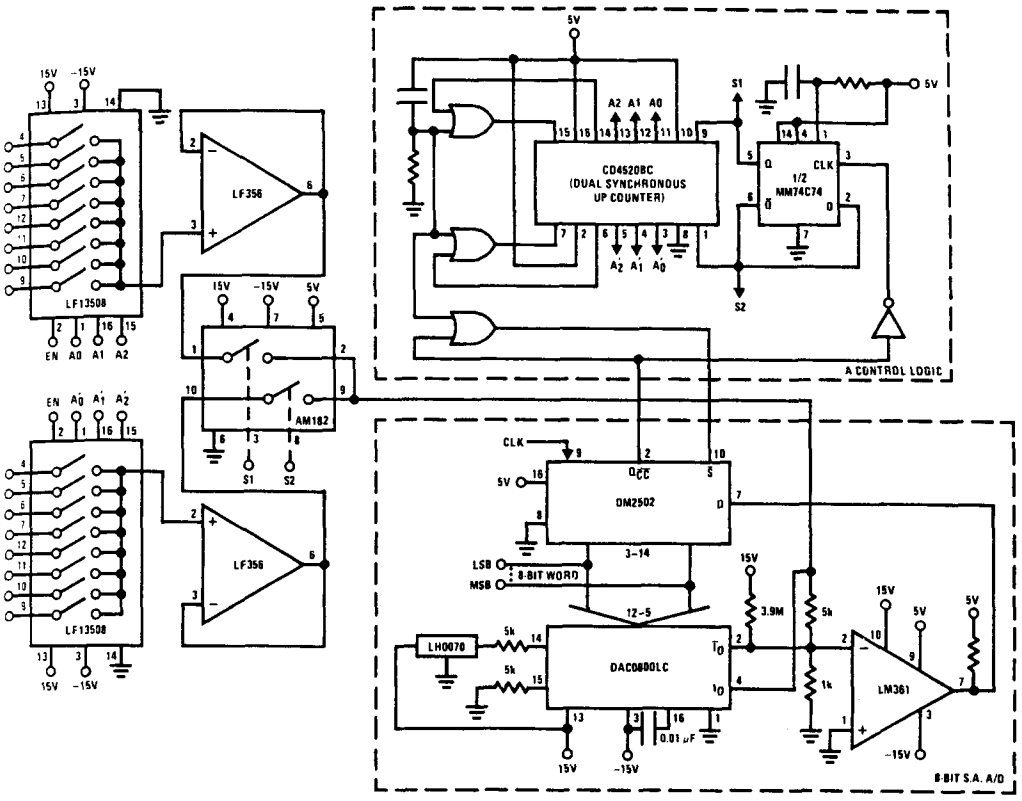

FIGURE 9a. A Fast 16-Channel DAU with Second Level Multiplexing

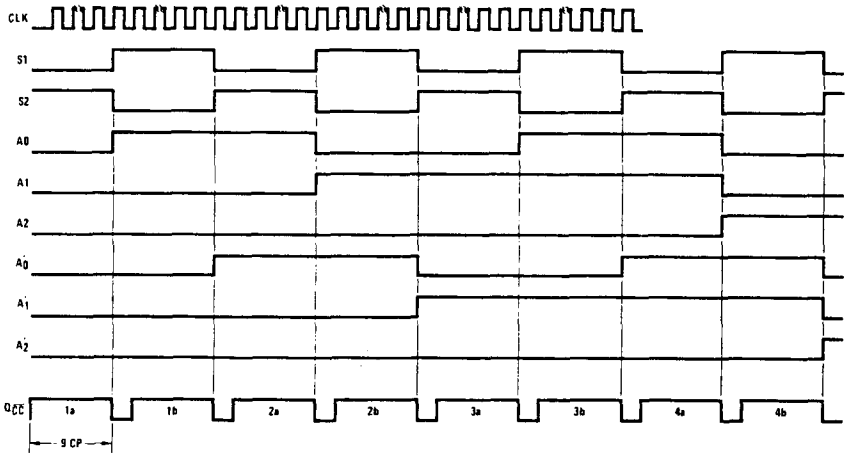

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FIGURE 9b. Timing Diagram

Typical Applications (Continued)

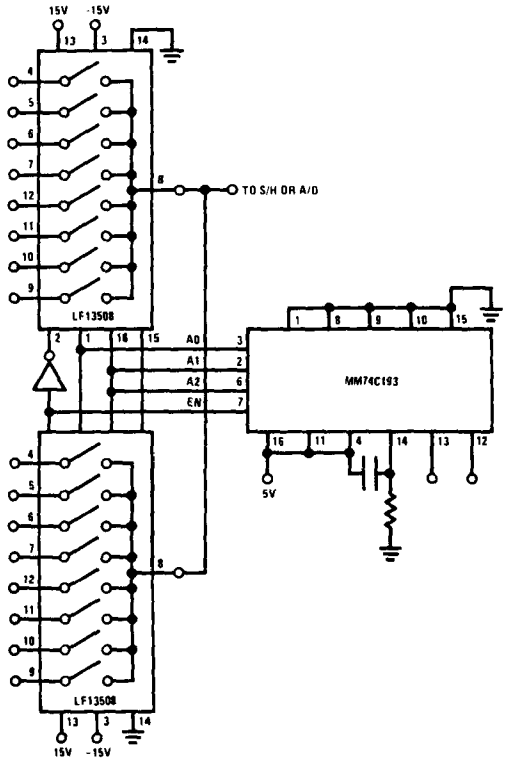

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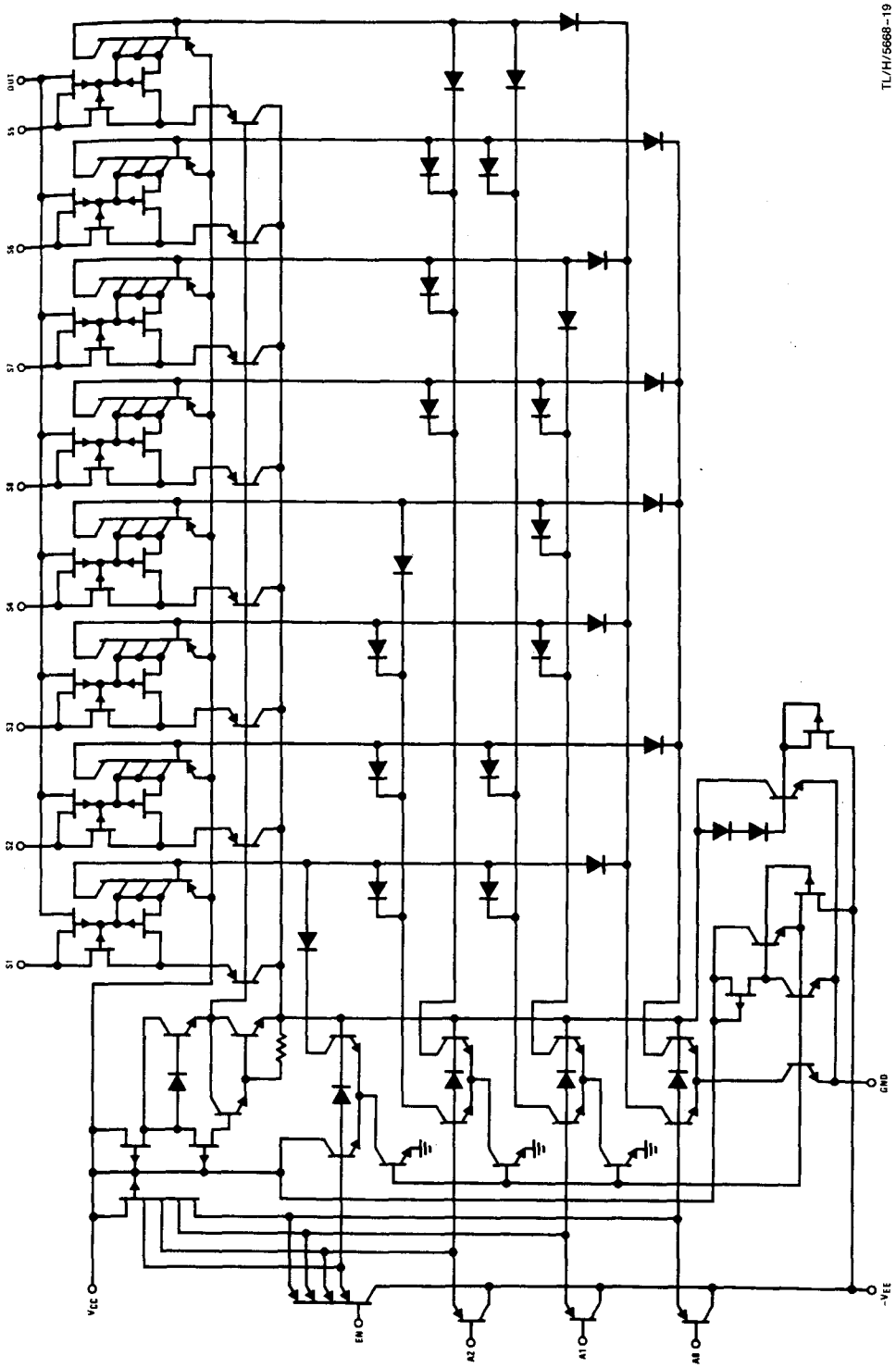
FIGURE 10. A 16-Channel Multiplexer with Sequential Multiplexing

Schematic Diagrams

LF13508



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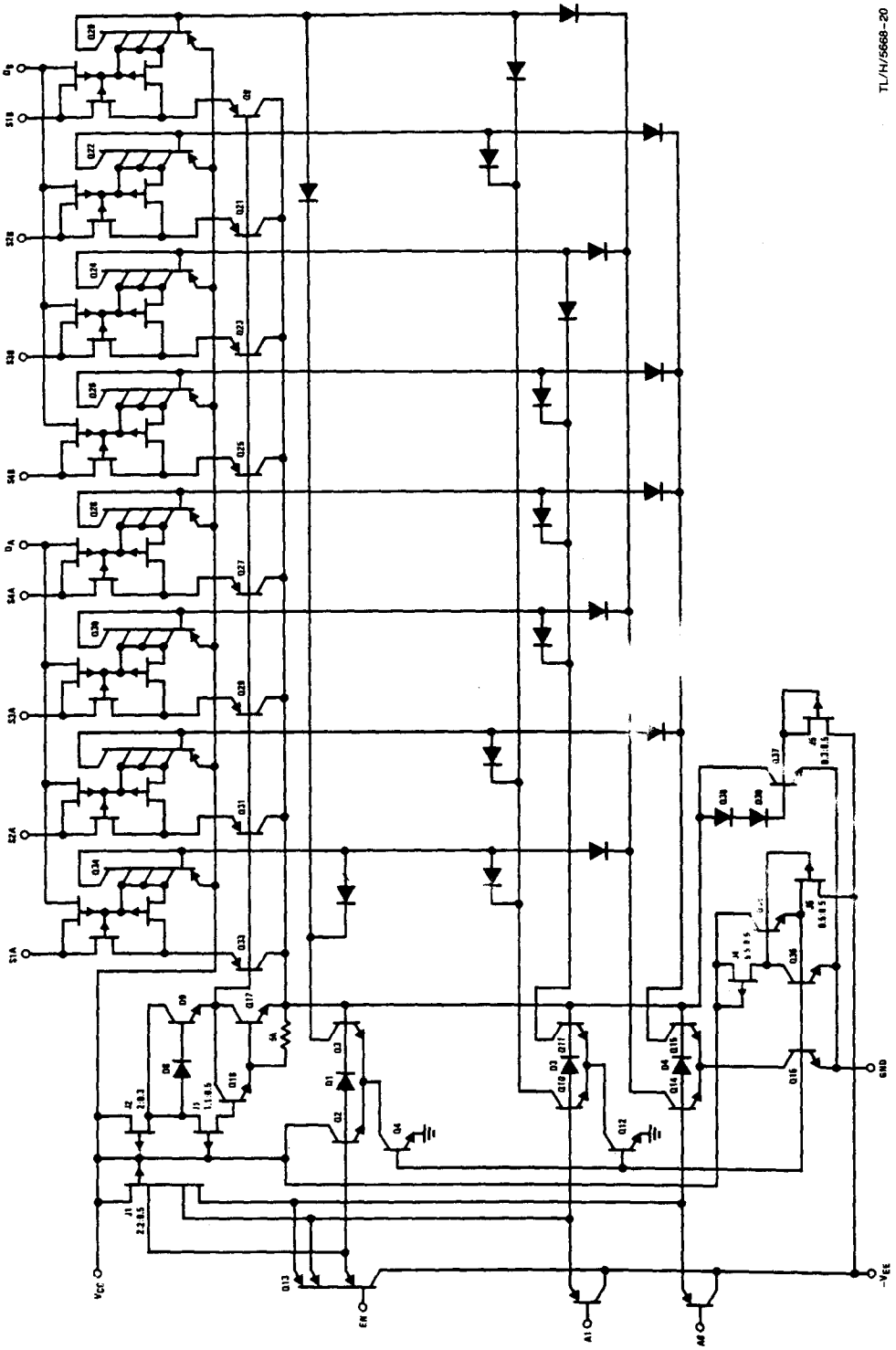
Schematic Diagrams (Continued)

LF13509



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