Low Noise, High Frequency, 8th Order Linear Phase Lowpass Filter

FEATURES

- 8th Order Filter in a 14-Pin Package
- 95kHz Maximum Corner Frequency
- No External Components
- 75:1, 150:1, and 120:1 Clock to Cutoff Frequency Ratio
- $60\mu V_{RMS}$ Total Wideband Noise
- 0.03% THD or Better
- Operates from ±2.37V to ±8V Power Supplies
- Low Total Output DC Offset

APPLICATIONS

- Antialiasing Filters
- Smoothing Filters
- Tracking High Frequency Lowpass Filters

DESCRIPTION

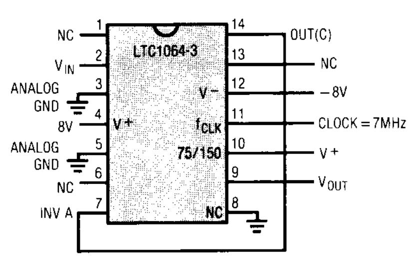
The LTC1064-3 is a monolithic 8th order lowpass Bessel filter, which provides a linear phase response over its entire passband. An external TTL or CMOS clock programs the filter's cutoff frequency. The clock to cutoff frequency ratio is 75:1 (pin 10 at V^+) or 150:1 (pin 10 at V^-) or 120:1 (pin 10 at GND). The maximum cutoff frequency is 95kHz. No external components are needed.

The LTC1064-3 features low wideband noise and low harmonic distortion even for input voltages up to $3V_{RMS}$. In fact the LTC1064-3 overall performance competes with equivalent multiple op amp RC active realizations. The LTC1064-3 is available in a 14-pin DIP or 16-pin surface mounted SOL package. The LTC1064-3 is fabricated using LTC's enhanced analog CMOS Si-gate process.

The LTC1064-3 is pin compatible with the LTC1064-1, -2, and -4.

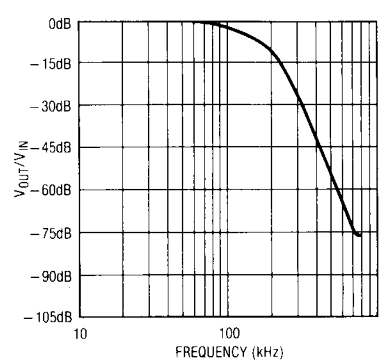
TYPICAL APPLICATION

8th Order Clock Sweepable Lowpass Bessel Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF OR LARGER CAPACITOR CLOSE TO THE PACKAGE. THE CONNECTION BETWEEN PINS 7 AND 14 SHOULD BE MADE UNDER THE I.C. PACKAGE.

Measured Frequency Response

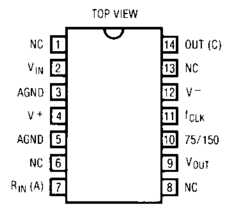


$V_S = \pm 7.5V$, $f_{CLK} = 7MHz$, PIN 10 TO V+, $f_{-3dB} = 95kHz$, GROUP DELAY = 6µs

ABSOLUTE MAXIMUM RATINGS

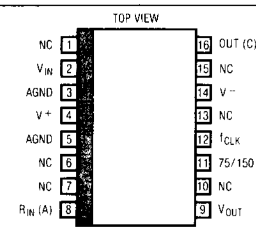
Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C
Operating Temperature Range
LTC1064-3M .... −55°C to 125°C
LTC1064-3C .... −40°C to 85°C
Input Voltage .... (V^+ + 0.3V) to (V^- − 0.3V)
Burn-In Voltage 15V

PACKAGE/ORDER INFORMATION



J PACKAGE 14-LEAD CERAMIC DIP　N PACKAGE 14-LEAD PLASTIC DIP

ORDER PART NUMBER
LTC1064-3MJ
LTC1064-3CJ
LTC1064-3CN



S PACKAGE 16-LEAD PLASTIC SOL

ORDER PART NUMBER
LTC1064-3CS

ELECTRICAL CHARACTERISTICS

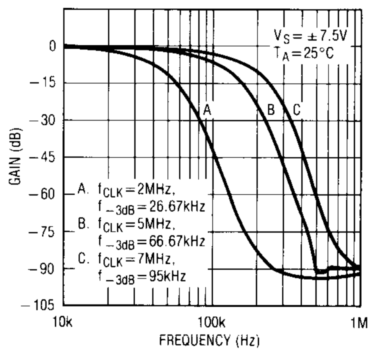
V_S = ±7.5V, 75:1, f_{CLK} = 2MHz, R_l = 10kΩ, T_A = 25°, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	Referenced to 0dB, 1Hz to 1kHz	●	−0.5		0.15	dB
Gain TempCo				0.0002		dB/°C
−3dB Frequency	50:1 (f_{CLK}/f_{-3dB} = 75)			26.67		kHz
	100:1 (f_{CLK}/f_{-3dB} = 150)			13.34		kHz
Gain at −3dB Frequency	Ref. to 0dB, f_{IN} = 26.67/13.34kHz	●	−3.8		−2.75	dB
Stopband Attenuation	At $3f_{-3dB}$	●	−25	−29		dB
Stopband Attenuation	At $5f_{-3dB}$	●	−56	−60		dB
Stopband Attenuation	At $7f_{-3dB}$			−84		dB
Input Frequency Range	100:1		0		$<f_{CLK}/2$	kHz
	50:1		0		$<f_{CLK}$	kHz
Output Voltage Swing and Operating Input Voltage Range	V_S = ±2.37V	●	±1.1			V
	V_S = ±5V	●	±3.1			V
	V_S = ±7.5V	●	±5.1			V
Total Harmonic Distortion	V_S = ±5V, Input = $1V_{RMS}$ at 1kHz			0.015		%
	V_S = ±7.5V, Input = $3V_{RMS}$ at 1kHz			0.03		%
Wideband Noise	V_S = ±5V, Input = GND 1Hz-1.99MHz			55		μV_{RMS}
	V_S = ±7.5V, Input = GND 1Hz-1.99MHz			60		μV_{RMS}
Output DC Offset	V_S = ±7.5V			±30	±150	mV
Output DC Offset TempCo	V_S = ±5V			±20		μV/°C
	V_S = ±7.5V			±50		μV/°C
Input Impedance			14	22		kΩ
Output Impedance	f_{OUT} = 10kHz			2		Ω
Output Short Circuit Current	Source/Sink			3/1		mA
Clock Feedthrough				200		μV_{RMS}
Maximum Clock Frequency	V_S > ±7V 50% Duty Cycle				5	MHz
	V_S > ±7V 50% Duty Cycle, T_A < 55°C				7	MHz
Power Supply Current	V_S = ±2.37V, f_{CLK} = 1MHz	●		10	18	mA
	V_S = ±5V, f_{CLK} = 1MHz			12	20	mA
		●			24	mA
	V_S = ±7.5V, f_{CLK} = 1MHz			16	24	mA
		●			32	mA
Power Supply Voltage Range		●	±2.37		±8	V

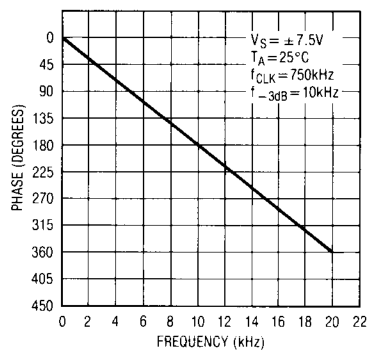
The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

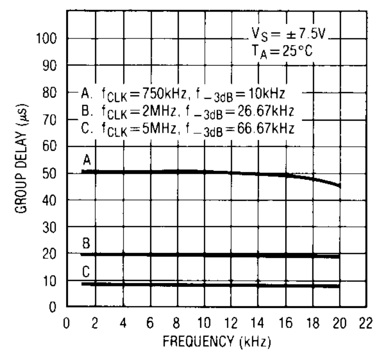
Graph 1. Gain vs Frequency



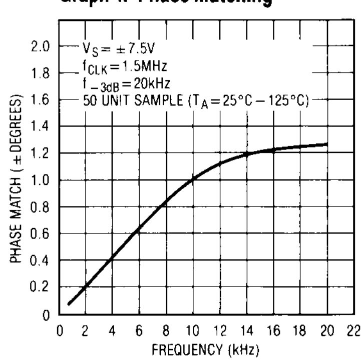
Graph 2. Phase vs Frequency



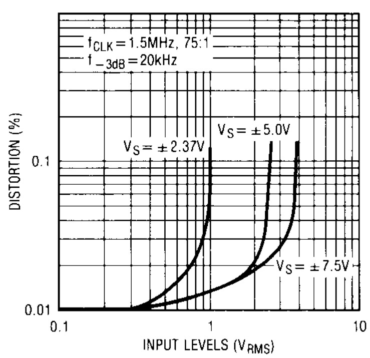
Graph 3. Group Delay



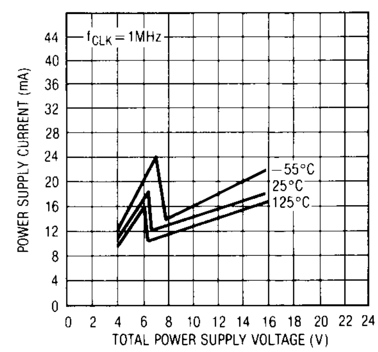
Graph 4. Phase Matching



Graph 5. Total Harmonic Distortion



Graph 6. Power Supply Current vs Power Supply Voltage



Graph 7. Transient Response Input 10Vp-p Square Wave $V_S = \pm 7.5V$, Pin 10 to V^+, $f_{CLK} = 1.5MHz$

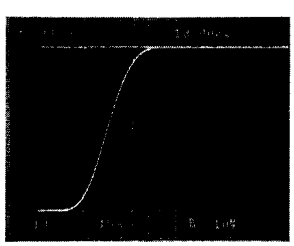


Table 1. Wideband Noise (μV_{RMS})

PIN 10 TO	f_{CLK}/f_{-3dB}	$V_S = \pm 2.37V$ NOISE μV_{RMS}	$V_S = \pm 5V$ NOISE μV_{RMS}	$V_S = \pm 7.5V$ NOISE μV_{RMS}
V^+	75/1	50	55	60
V^-	150/1	52	58	62
GND	120/1	45	50	54

TYPICAL PERFORMANCE CHARACTERISTICS

Table 2. Gain/Phase, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C f_{CLK} = 75kHz, Pin 10 at V^+ (fltr 75:1)

FREQUENCY	GAIN	PHASE
0.500kHz	−0.858dB	−90.430 deg
1.000kHz	−2.990dB	179.200 deg
1.500kHz	−6.840dB	89.600 deg
2.000kHz	−12.780dB	3.800 deg
2.500kHz	−20.800dB	−71.000 deg
3.000kHz	−29.900dB	−129.600 deg
3.500kHz	−38.800dB	−173.700 deg
4.000kHz	−47.100dB	152.600 deg
4.500kHz	−54.700dB	126.000 deg
5.000kHz	−61.600dB	103.300 deg
5.500kHz	−68.000dB	85.190 deg
6.000kHz	−73.840dB	69.060 deg
6.500kHz	−79.250dB	54.780 deg
7.000kHz	−84.230dB	42.440 deg
7.500kHz	−88.940dB	30.060 deg
8.000kHz	−93.360dB	21.300 deg
8.500kHz	−97.510dB	10.000 deg
9.000kHz	−100.880dB	1.520 deg
9.500kHz	−105.780dB	−7.820 deg

Table 3. Gain/Delay, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C f_{CLK} = 75kHz, Pin 10 at V^+ (fltr 75:1)

FREQUENCY	GAIN	DELAY
0.200kHz	−0.281dB	0.502ms
0.300kHz	−0.420dB	0.503ms
0.400kHz	−0.610dB	0.503ms
0.500kHz	−0.860dB	0.502ms
0.600kHz	−1.160dB	0.502ms
0.700kHz	−1.530dB	0.502ms
0.800kHz	−1.950dB	0.503ms
0.900kHz	−2.430dB	0.503ms
1.000kHz	−2.990dB	0.500ms
1.100kHz	−3.610dB	0.500ms
1.200kHz	−4.300dB	0.500ms
1.300kHz	−5.060dB	0.498ms
1.400kHz	−5.920dB	0.495ms
1.500kHz	−6.830dB	0.491ms
1.600kHz	−7.840dB	0.489ms
1.700kHz	−8.930dB	0.481ms
1.800kHz	−10.130dB	0.473ms
1.900kHz	−11.410dB	0.465ms
2.000kHz	−12.780dB	0.454ms

Table 4. Gain/Phase, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C f_{CLK} = 150kHz, Pin 10 at V^- (fltr 150:1)

FREQUENCY	GAIN	PHASE
0.500kHz	−0.955dB	−88.100 deg
1.000kHz	−3.380dB	−175.300 deg
1.500kHz	−7.570dB	99.700 deg
2.000kHz	−13.770dB	20.100 deg
2.500kHz	−21.800dB	−48.000 deg
3.000kHz	−30.700dB	−100.700 deg
3.500kHz	−39.400dB	−139.900 deg
4.000kHz	−47.600dB	−169.200 deg
4.500kHz	−55.100dB	168.300 deg
5.000kHz	−61.900dB	150.300 deg
5.500kHz	−68.260dB	135.830 deg
6.000kHz	−74.050dB	123.660 deg
6.500kHz	−79.450dB	113.440 deg
7.000kHz	−84.330dB	104.440 deg
7.500kHz	−89.010dB	97.670 deg
8.000kHz	−93.250dB	91.580 deg
8.500kHz	−97.340dB	84.670 deg
9.000kHz	−101.390dB	74.600 deg
9.500kHz	−104.980dB	75.990 deg

Table 5. Gain/Delay, f_{-3dB} = 1kHz, LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C f_{CLK} = 150kHz, Pin 10 at V^- (fltr 150:1)

FREQUENCY	GAIN	DELAY
0.200kHz	−0.284dB	0.490ms
0.300kHz	−0.450dB	0.489ms
0.400kHz	−0.670dB	0.489ms
0.500kHz	−0.960dB	0.487ms
0.600kHz	−1.310dB	0.487ms
0.700kHz	−1.730dB	0.485ms
0.800kHz	−2.210dB	0.484ms
0.900kHz	−2.750dB	0.482ms
1.000kHz	−3.380dB	0.478ms
1.100kHz	−4.070dB	0.478ms
1.200kHz	−4.820dB	0.475ms
1.300kHz	−5.660dB	0.470ms
1.400kHz	−6.580dB	0.467ms
1.500kHz	−7.570dB	0.463ms
1.600kHz	−8.640dB	0.456ms
1.700kHz	−9.790dB	0.448ms
1.800kHz	−11.050dB	0.438ms
1.900kHz	−12.360dB	0.428ms
2.000kHz	−13.770dB	0.417ms

TYPICAL PERFORMANCE CHARACTERISTICS

Table 6. Gain/Phase, f_{-3dB} = 1kHz,
LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C
f_{CLK} = 120kHz, Pin 10 at GND (fltr 120:1)

FREQUENCY	GAIN	PHASE
0.500kHz	−0.994dB	−82.210 deg
1.000kHz	−3.050dB	−162.800 deg
1.500kHz	−6.520dB	116.700 deg
2.000kHz	−12.180dB	40.200 deg
2.500kHz	−19.460dB	−23.600 deg
3.000kHz	−27.200dB	−74.000 deg
3.500kHz	−34.700dB	−114.200 deg
4.000kHz	−41.900dB	−146.800 deg
4.500kHz	−48.700dB	−173.300 deg
5.000kHz	−55.100dB	164.700 deg
5.500kHz	−60.900dB	145.800 deg
6.000kHz	−66.500dB	130.610 deg
6.500kHz	−71.660dB	117.130 deg
7.000kHz	−76.390dB	105.880 deg
7.500kHz	−80.910dB	96.140 deg
8.000kHz	−84.900dB	87.510 deg
8.500kHz	−88.750dB	81.380 deg
9.000kHz	−92.410dB	78.190 deg
9.500kHz	−98.290dB	52.860 deg

Table 7. Gain/Delay, f_{-3dB} = 1kHz,
LTC1064-3 Typical Response V_S = ±5V, T_A = 25°C
f_{CLK} = 120kHz, Pin 10 at GND (fltr 120:1)

FREQUENCY	GAIN	DELAY
0.200kHz	−0.354dB	0.458ms
0.300kHz	−0.520dB	0.456ms
0.400kHz	−0.730dB	0.454ms
0.500kHz	−1.000dB	0.452ms
0.600kHz	−1.320dB	0.449ms
0.700kHz	−1.670dB	0.448ms
0.800kHz	−2.090dB	0.446ms
0.900kHz	−2.540dB	0.446ms
1.000kHz	−3.050dB	0.445ms
1.100kHz	−3.600dB	0.446ms
1.200kHz	−4.220dB	0.449ms
1.300kHz	−4.900dB	0.448ms
1.400kHz	−5.670dB	0.447ms
1.500kHz	−6.520dB	0.446ms
1.600kHz	−7.470dB	0.441ms
1.700kHz	−8.500dB	0.432ms
1.800kHz	−9.650dB	0.422ms
1.900kHz	−10.870dB	0.409ms
2.000kHz	−12.180dB	0.395ms

Table 8. Gain/Phase, f_{-3dB} = 20kHz,
LTC1064-3 Typical Response V_S = ±7.5V,
f_{CLK} = 1.5MHz, Pin 10 at V^+ (fltr 75:1)

T_A = 25°C

FREQUENCY	GAIN	PHASE
10.000kHz	−0.912dB	−92.270 deg
20.000kHz	−3.090dB	176.000 deg
30.000kHz	−6.910dB	85.500 deg
40.000kHz	−12.710dB	−1.200 deg
50.000kHz	−20.500dB	−77.800 deg
60.000kHz	−29.400dB	−138.700 deg
70.000kHz	−38.300dB	174.600 deg
80.000kHz	−46.500dB	138.300 deg
90.000kHz	−54.000dB	109.100 deg
100.000kHz	−61.000dB	84.800 deg
110.000kHz	−67.310dB	64.040 deg
120.000kHz	−73.170dB	46.260 deg
130.000kHz	−78.600dB	31.120 deg
140.000kHz	−83.760dB	18.050 deg
150.000kHz	−88.630dB	7.770 deg

T_A = 125°C

FREQUENCY	GAIN	PHASE
10.000kHz	−0.944dB	−92.880 deg
20.000kHz	−3.170dB	175.500 deg
30.000kHz	−6.910dB	85.700 deg
40.000kHz	−12.450dB	−0.600 deg
50.000kHz	−19.920dB	−78.000 deg
60.000kHz	−28.500dB	−140.700 deg
70.000kHz	−37.200dB	170.500 deg
80.000kHz	−45.300dB	132.200 deg
90.000kHz	−52.700dB	100.900 deg
100.000kHz	−59.600dB	74.900 deg
110.000kHz	−65.900dB	52.600 deg
120.000kHz	−71.750dB	32.850 deg
130.000kHz	−77.170dB	15.840 deg
140.000kHz	−82.370dB	1.130 deg
150.000kHz	−87.400dB	−11.380 deg

PIN DESCRIPTION

Power Supply Pins (4, 12)

The V^+ (pin 4) and V^- (pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. Low noise, non-switching power supplies are recommended. **To avoid latch up when the power supplies exhibit high turn-on transients, a 1N5817 schottky diode should be added from the V^+ and V^- pins to ground, Figures 1, 2 and 3.**

Clock Pin (11)

For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are 2.2V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 7MHz. Do not allow the clock levels to exceed the power supplies. For single supply operation ≥6V use level shifting at pin 11 with T^2L levels, see Figure 4.

Analog Ground Pins (3, 5)

For dual supply operation these pins should be connected to a ground plane. For single supply operation both pins should be tied to one half supply, Figure 3.

Connection Pins (7, 14)

A very short connection between pins 14 and 7 is recommended. This connection should be preferably done under the IC package. In a breadboard, use a one inch, or less, shielded coaxial cable; the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

Input, Output Pins (2, 9)

The input pin 2 is connected to an 18kΩ resistor tied to the inverting input of an op amp. Pin 2 is protected against static discharge. The device's output, pin 9, is the output of an op amp which can typically source/sink 3/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, pin 9, should be buffered, Figure 1. **The op amp power supply wire (or trace) should be connected directly to the power source. To eliminate switching transients from filter output, buffer filter output with a third order lowpass, see Figure 5.**

NC Pins (1, 6, 8, 13)

The "no connection" pins should be preferably grounded. These pins are not internally connected.

Ratio Pin (10)

The DC level at this pin determines the ratio of clock frequency to the −3dB frequency of the filter. The ratio is 75:1 when pin 10 is at V^+, 120:1 when pin 10 is at GND and 150:1 when pin 10 is at V^-. This pin should be bypassed with a 0.1µF capacitor to analog ground when it's connected to V^- or V^+, Figure 1. See Tables 2 through 8 for typical gain, phase and delay responses for the three ratios.

PIN DESCRIPTION

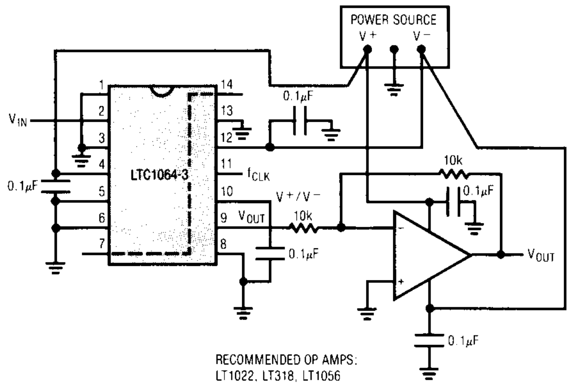


Figure 1. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-3 Power Lines.

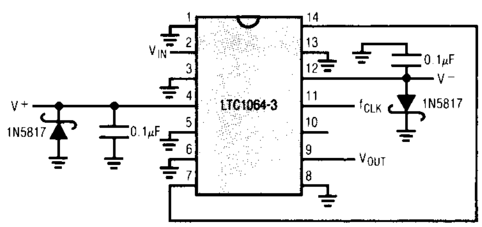


Figure 2. Using Schottky Diodes to Protect the IC from Transient Supply Reversal.

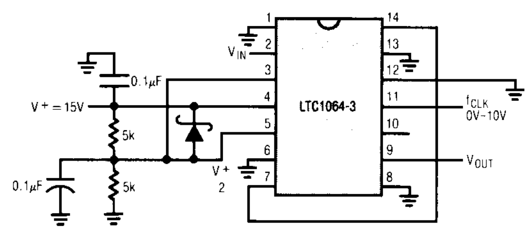


Figure 3. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pins 4 and 5.

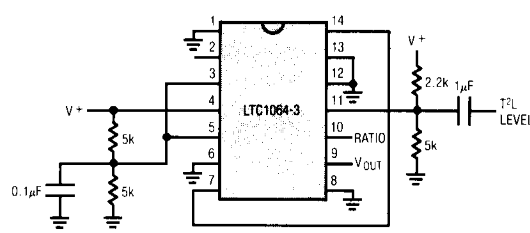


Figure 4. Level Shifting the Input T²L Clock for Single Supply Operation ≥ 6V.

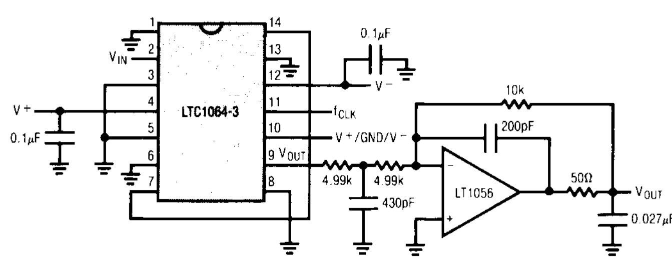
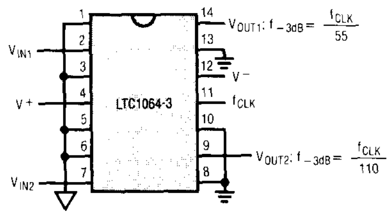


Figure 5. Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough. Passband ±0.1dB to 50kHz, −3dB at 94kHz.

TYPICAL APPLICATION



Amplitude Response

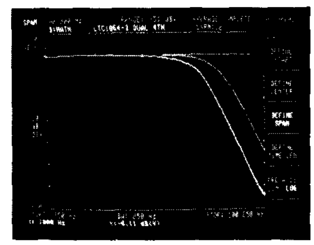
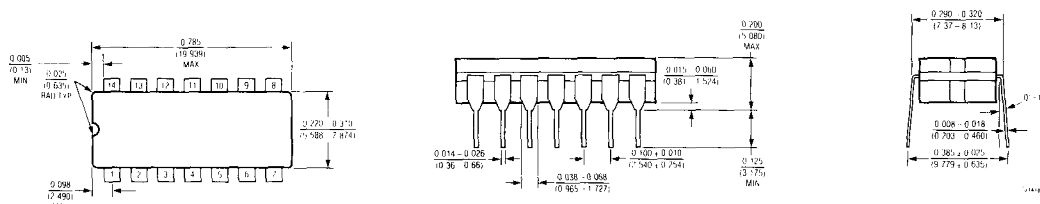


Figure 6. Dual 4th Order Bessel Filters. $V_S = \pm 7.5V$, $f_{CLK} = 1MHz$, Pin 10 to GND. f_{-3dB} = 9kHz and 18kHz.

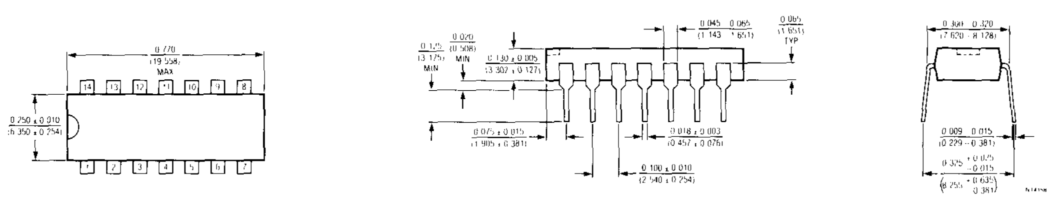
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

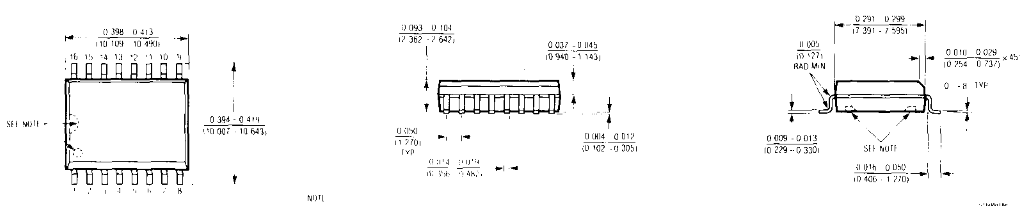
J Package
14-Lead Ceramic DIP



N Package
14-Lead Plastic DIP



S Package
16-Lead Plastic SOL



NOTE:
PIN 1 IDENT. NOTCH ON TOP AND CAVITIES
ON THE BOTTOM OF PACKAGE ARE THE
MANUFACTURING OPTIONS. THE PART
MAY BE SUPPLIED WITH OR WITHOUT
ANY OF THE OPTIONS.

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