National Semiconductor

MF6 6th Order Switched Capacitor
Butterworth Lowpass Filter

General Description
The MF6 is a versatile easy to use, precision 6th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF6-50) or 100 to 1 (MF6-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or an external TTL or CMOS logic compatible clock can be used for tighter cutoff frequency control. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF6 sections for higher order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications.

Features
- No external components
- 14-pin DIP or 14-pin wide-body S.O. package
- Cutoff frequency accuracy of ± 0.3% typical
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Two uncommitted op amps available
- 5V to 14V total supply voltage
- Cutoff frequency set by external or internal clock

Block and Connection Diagrams

All Packages

N. INVZ 1
14. INVZ
13. INVY
12. INVX
11. CLX X
10. "V+
9. "V-
8. CLX M
7. CLX S
6. VCC
5. VEE
4. GND

Order Number MF6CWM-50 or MF6CWM-100
See NS Package Number M14B
Order Number MF6CN-50 or MF6CN-100
See NS Package Number N14A
Order Number MF6CJ-50 or MF6CJ-100
See NS Package Number J14A

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### Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage: 14V
- Voltage at Any Pin: $V^+ = -0.2V, V^- + 0.2V$
- Input Current at Any Pin (Note 13): 5 mA
- Package Input Current (Note 13): 20 mA
- Power Dissipation (Note 14): 500 mW
- Storage Temperature: -65°C to +150°C
- ESD Susceptibility (Note 12): 800V
- Soldering Information:
  - N Package (10 sec.): 260°C
  - J Package (10 sec.): 300°C
  - SO Package: 215°C
  - Infrared (15 sec.): 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

### Operating Ratings (Note 11)

- Temperature Range:
  - MF6CN-50, MF6CN-100: $0°C \leq T_A \leq +70°C$
  - MF6CWM-50, MF6CWM-100: $0°C \leq T_A \leq +70°C$
  - MF6CJ-50, MF6CJ-100: $-40°C \leq T_A \leq +85°C$
- Supply Voltage ($V_S = V^+ - V^-$): 5V to 14V

### Filter Electrical Characteristics

The following specifications apply for $f_{CLK} \leq 250$ kHz (see Note 3) unless otherwise specified. Boldface limits apply for $T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_J = 25°C$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>MF6CWM-50, MF6CWM-100, MF6CN-50, MF6CN-100</th>
<th>MF6CJ-50, MF6CJ-100</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V^+ = +5V, V^- = -5V$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{Cutoff}$ MF6-50</td>
<td>Min</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency (Max)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Range MF6-100</td>
<td>Min</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Note 1)</td>
<td>Max</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Supply Current $f_{CLK} = 250$ kHz</td>
<td>4.0</td>
<td>6.0</td>
<td>8.5</td>
<td>4.0</td>
</tr>
<tr>
<td>Maximum Clock Filter Output</td>
<td>30</td>
<td>30</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Feedthrough Op Amp 1 Out</td>
<td>25</td>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Op Amp 2 Out</td>
<td>20</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{source}$</td>
<td>$\leq 2$ kΩ</td>
<td>0.0</td>
<td>±0.30</td>
<td>±0.30</td>
</tr>
<tr>
<td>$f_{CLK} / f_{Cutoff}$ MF6-50</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency Ratio MF6-100</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Voltage MF6-50</td>
<td>-200</td>
<td>-200</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>MF6-100</td>
<td>-400</td>
<td>-400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Output Voltage Swing</td>
<td>$+4.0$</td>
<td>$+3.5$</td>
<td>$+3.5$</td>
<td>$+4.0$</td>
</tr>
<tr>
<td>$R_L = 10$ kΩ</td>
<td>$-4.1$</td>
<td>$-3.8$</td>
<td>$-3.8$</td>
<td>$-4.1$</td>
</tr>
<tr>
<td>Maximum Output Short Circuit Constant Current (Note 6)</td>
<td>Source</td>
<td>50</td>
<td>60</td>
<td>80</td>
</tr>
<tr>
<td>Sink</td>
<td>1.5</td>
<td>2.0</td>
<td>3.0</td>
<td>1.5</td>
</tr>
<tr>
<td>Dynamic Range MF6-50 (Note 2)</td>
<td>83</td>
<td>83</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MF6-100</td>
<td>81</td>
<td>81</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Additional Magnitude</td>
<td>6000 Hz</td>
<td>-0.47</td>
<td>$-0.47 \pm 0.5$</td>
<td>$-0.47 \pm 0.65$</td>
</tr>
<tr>
<td>Response Test $f = 4500$ Hz</td>
<td>-0.92</td>
<td>$-0.92 \pm 0.2$</td>
<td>$-0.92 \pm 0.3$</td>
<td>-0.92</td>
</tr>
<tr>
<td>Points (Note 4)</td>
<td>MF6-50 $f_{CLK} = 250$ kHz</td>
<td>-0.48</td>
<td>$-0.48 \pm 0.5$</td>
<td>$-0.48 \pm 0.65$</td>
</tr>
<tr>
<td>MF6-100</td>
<td>-0.97</td>
<td>$-0.97 \pm 0.2$</td>
<td>$-0.97 \pm 0.3$</td>
<td>-0.97</td>
</tr>
</tbody>
</table>
Filter Electrical Characteristics (Continued) The following specifications apply for \( f_{\text{CLK}} \leq 250 \) kHz (see Note 3) unless otherwise specified. **Boldface limits apply for \( T_{\text{MIN}} \) to \( T_{\text{MAX}} \); all other terms \( T_A = T_J = 25^\circ \text{C} \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>MF6CWM-50, MF6CWM-100</th>
<th>MF6CN-50, MF6CN-100</th>
<th>MF6CJ-50, MF6CJ-100</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Typical (Note 8)</td>
<td>Tested Limit (Note 9)</td>
<td>Design Limit (Note 10)</td>
</tr>
<tr>
<td>( V^+ = +5\text{V}, V^- = -5\text{V} ) (Continued)</td>
<td>MF6-50</td>
<td>( f_{\text{CLK}} = 250 ) kHz ( f_1 = 6000 \text{Hz} ) ( f_2 = 8000 \text{Hz} )</td>
<td>-36</td>
<td>-36</td>
</tr>
<tr>
<td>Attenuation Rate</td>
<td>MF6-100</td>
<td>( f_{\text{CLK}} = 250 ) kHz ( f_1 = 3000 \text{Hz} ) ( f_2 = 4000 \text{Hz} )</td>
<td>-36</td>
<td>-36</td>
</tr>
<tr>
<td>( V^+ = +2.5\text{V}, V^- = -2.5\text{V} )</td>
<td>MF6-50</td>
<td>Minimum Cutoff Frequency ( f_{\text{C}} )</td>
<td>0.1</td>
<td>10k</td>
</tr>
<tr>
<td>Initial</td>
<td>Maximum</td>
<td>Frequency</td>
<td>( f_{\text{C}} )</td>
<td>( 0.1 \text{kHz} )</td>
</tr>
<tr>
<td>Frequency</td>
<td>( f_{\text{C}} )</td>
<td>( f_{\text{C}} )</td>
<td>( f_{\text{C}} )</td>
<td>( f_{\text{C}} )</td>
</tr>
<tr>
<td>Range</td>
<td>MF6-100</td>
<td>2.5</td>
<td>4.0</td>
<td>4.0</td>
</tr>
<tr>
<td>Total Supply Current</td>
<td>( f_{\text{CLK}} = 250 ) kHz</td>
<td>20</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>Maximum Clock Feedthrough</td>
<td>Op Amp 1 Out</td>
<td>0.0</td>
<td>±0.30</td>
<td>±0.30</td>
</tr>
<tr>
<td>Op Amp 2 Out</td>
<td>20</td>
<td>15</td>
<td>10</td>
<td>0.0</td>
</tr>
<tr>
<td>DC Offset Voltage</td>
<td>MF6-50</td>
<td>49.10 ± 0.3%</td>
<td>49.10 ± 2%</td>
<td>49.10 ± 3%</td>
</tr>
<tr>
<td>MF6-100</td>
<td>98.65 ± 0.3%</td>
<td>98.65 ± 2%</td>
<td>98.65 ± 2.25%</td>
<td>98.65 ± 0.3%</td>
</tr>
<tr>
<td>H\sub{2}, DC Gain</td>
<td>( R_{\text{source}} = 2 ) k\text{\Omega}</td>
<td>0.0</td>
<td>±0.30</td>
<td>±0.30</td>
</tr>
<tr>
<td>( f_{\text{CLK}} / f_{\text{C}}, \text{Clock-to-Cutoff Frequency} )</td>
<td>MF6-50</td>
<td>49.10 ± 0.3%</td>
<td>49.10 ± 2%</td>
<td>49.10 ± 3%</td>
</tr>
<tr>
<td>MF6-100</td>
<td>98.65 ± 0.3%</td>
<td>98.65 ± 2%</td>
<td>98.65 ± 2.25%</td>
<td>98.65 ± 0.3%</td>
</tr>
<tr>
<td>DC Offset Voltage</td>
<td>MF6-50</td>
<td>-200</td>
<td>-400</td>
<td>mV</td>
</tr>
<tr>
<td>MF6-100</td>
<td>-200</td>
<td>-400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Output Voltage Swing</td>
<td>( R_L = 10 ) k\text{\Omega}</td>
<td>+1.5</td>
<td>+1.0</td>
<td>+1.0</td>
</tr>
<tr>
<td>Voltage Swing</td>
<td>MF6-50</td>
<td>-2.2</td>
<td>-1.7</td>
<td>-1.5</td>
</tr>
<tr>
<td>MF6-100</td>
<td>-2.2</td>
<td>-1.7</td>
<td>-1.5</td>
<td>-2.2</td>
</tr>
<tr>
<td>Maximum Output Source Current (Note 6)</td>
<td>( f_{\text{CLK}} = 250 ) kHz</td>
<td>28</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>Short Circuit Current (Note 6)</td>
<td>( f_{\text{CLK}} = 250 ) kHz</td>
<td>0.5</td>
<td>1.0</td>
<td>1.5</td>
</tr>
<tr>
<td>Dynamic Range (Note 2)</td>
<td>MF6-50</td>
<td>77</td>
<td>77</td>
<td>dB</td>
</tr>
<tr>
<td>MF6-100</td>
<td>95.4 ± 0.5</td>
<td>95.4 ± 0.5</td>
<td>95.4 ± 0.65</td>
<td>95.4 ± 0.65</td>
</tr>
<tr>
<td>Additional Magnitude</td>
<td>MF6-100</td>
<td>-0.96</td>
<td>-0.96</td>
<td>-0.96</td>
</tr>
<tr>
<td>MF6-100</td>
<td>-1.01</td>
<td>-1.01</td>
<td>-1.01</td>
<td>-1.01</td>
</tr>
<tr>
<td>Attenuation Rate</td>
<td>MF6-50</td>
<td>( f_{\text{CLK}} = 250 ) kHz ( f_1 = 6000 \text{Hz} ) ( f_2 = 8000 \text{Hz} )</td>
<td>-36</td>
<td>-36</td>
</tr>
<tr>
<td>MF6-100</td>
<td>( f_{\text{CLK}} = 250 ) kHz ( f_1 = 3000 \text{Hz} ) ( f_2 = 4000 \text{Hz} )</td>
<td>-36</td>
<td>-36</td>
<td>-36</td>
</tr>
</tbody>
</table>

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## Op Amp Electrical Characteristics

Boldface limits apply for $T_{\text{MIN}}$ to $T_{\text{MAX}}$; all other limits $T_A = T_J = 25^\circ C$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>MF6CN-50, MF6CN-100, MF6CWM-50, MF6CWM-100</th>
<th>MF6CJ-50, MF6CJ-100</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Typical (Note 8)</td>
<td>Tested Limit (Note 9)</td>
</tr>
<tr>
<td>$V^+ = +5V, V^- = -5V$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>$\pm 8.0$</td>
<td>$\pm 20$</td>
<td>$\mathbf{20}$</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>10</td>
<td>10</td>
<td>pA</td>
</tr>
<tr>
<td>OMRR (Op Amp #2 Only)</td>
<td>$V_{CM1} = 1.8V, V_{CM2} = -2.2V$</td>
<td>60</td>
<td>55</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_L = 10k\Omega$</td>
<td>$+4.0$</td>
<td>$+3.8$</td>
<td>$\mathbf{3.6}$</td>
</tr>
<tr>
<td>Maximum Output Short Circuit Current (Note 8)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Source</td>
<td>54</td>
<td>65</td>
<td>80</td>
</tr>
<tr>
<td>Sink</td>
<td>2.0</td>
<td>4.0</td>
<td>6.0</td>
</tr>
<tr>
<td>slew Rate</td>
<td>7.0</td>
<td>7.0</td>
<td>V/μs</td>
</tr>
<tr>
<td>DC Open Loop Gain</td>
<td>72</td>
<td>72</td>
<td>dB</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>1.2</td>
<td>1.2</td>
<td>MHz</td>
</tr>
<tr>
<td>$V^+ = +2.5V, V^- = -2.5V$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>$\pm 8.0$</td>
<td>$\pm 20$</td>
<td>$\mathbf{20}$</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>10</td>
<td>10</td>
<td>pA</td>
</tr>
<tr>
<td>OMRR (Op-Amp #2 Only)</td>
<td>$V_{CM1} = +0.5V, V_{CM2} = -0.9V$</td>
<td>60</td>
<td>55</td>
</tr>
<tr>
<td>Output Voltage Swing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_L = 10k\Omega$</td>
<td>$+1.5$</td>
<td>$+1.3$</td>
<td>$+1.1$</td>
</tr>
<tr>
<td>Maximum Output Short Circuit Current (Note 8)</td>
<td></td>
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</tr>
<tr>
<td>Source</td>
<td>24</td>
<td>35</td>
<td>50</td>
</tr>
<tr>
<td>Sink</td>
<td>1.0</td>
<td>2.0</td>
<td>4.0</td>
</tr>
<tr>
<td>slew Rate</td>
<td>6.0</td>
<td>6.0</td>
<td>V/μs</td>
</tr>
<tr>
<td>DC Open Loop Gain</td>
<td>67</td>
<td>67</td>
<td>dB</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>1.2</td>
<td>1.2</td>
<td>MHz</td>
</tr>
</tbody>
</table>
**Logic Input-Output Electrical Characteristics**

The following specifications apply for $V^* = 0$ V (see Note 5) unless otherwise specified. Boldface limits apply for $T_{MIN}$ to $T_{MAX}$; all other limits $T_A = T_J = 25^\circ C$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>MF56CN-50, MF56CN-100</th>
<th>MF56CWM-50, MF56CWM-100</th>
<th>MF56CJ-50, MF56CJ-100</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Typical (Note 8)</td>
<td>Tested Limit (Note 9)</td>
<td>Design Limit (Note 10)</td>
</tr>
<tr>
<td>TTL CLOCK INPUT, CLK R PIN (Note 7)</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum $V_{IL}$, Logical &quot;0&quot; Input Voltage</td>
<td></td>
<td>0.8</td>
<td>0.8</td>
<td></td>
</tr>
<tr>
<td>Minimum $V_{IH}$, Logical &quot;1&quot; Input Voltage</td>
<td></td>
<td>2.0</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>Maximum Leakage Current at CLK R Pin</td>
<td>L Sh Pin at Mid- Supply</td>
<td>2.0</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>SCHMITT TRIGGER</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>$V_{TH+}$, Positive Going Threshold Voltage</td>
<td>Min</td>
<td>V* = 10V</td>
<td>7.0</td>
<td>6.1</td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td></td>
<td>8.9</td>
<td>8.9</td>
</tr>
<tr>
<td></td>
<td>Min</td>
<td>V* = 5V</td>
<td>3.5</td>
<td>3.1</td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td></td>
<td>4.4</td>
<td>4.4</td>
</tr>
<tr>
<td>$V_{TH-}$, Negative Going Threshold Voltage</td>
<td>Min</td>
<td>V* = 10V</td>
<td>3.0</td>
<td>1.3</td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td></td>
<td>3.8</td>
<td>3.8</td>
</tr>
<tr>
<td></td>
<td>Min</td>
<td>V* = 5V</td>
<td>1.5</td>
<td>0.6</td>
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<tr>
<td></td>
<td>Max</td>
<td></td>
<td>1.9</td>
<td>1.9</td>
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<tr>
<td>Hysteresis ($V_{TH+} - V_{TH-}$)</td>
<td>Min</td>
<td>V* = 10V</td>
<td>4.0</td>
<td>2.3</td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td></td>
<td>7.6</td>
<td>7.6</td>
</tr>
<tr>
<td></td>
<td>Min</td>
<td>V* = 5V</td>
<td>2.0</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>Max</td>
<td></td>
<td>3.8</td>
<td>3.8</td>
</tr>
<tr>
<td>Minimum Logical &quot;1&quot; Output Voltage (Pin 11)</td>
<td>I0 = -10mA</td>
<td>V* = 10V</td>
<td>9.0</td>
<td>9.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V* = 5V</td>
<td>4.5</td>
<td>4.5</td>
</tr>
<tr>
<td></td>
<td>I0 = 10mA</td>
<td>V* = 10V</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V* = 5V</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Minimum Output Source Current (Pin 11)</td>
<td>CLK R Tied to Ground</td>
<td>V* = 10V</td>
<td>6.0</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V* = 5V</td>
<td>1.5</td>
<td>0.75</td>
</tr>
<tr>
<td>Maximum Output Sink Current (Pin 11)</td>
<td>CLK R Tied to $V^*$</td>
<td>V* = 10V</td>
<td>5.0</td>
<td>2.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V* = 5V</td>
<td>1.3</td>
<td>0.65</td>
</tr>
</tbody>
</table>

**Note 1:** The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3 dB below the DC gain of the filter.

**Note 2:** For ±5 V supplies the dynamic range is referenced to ±82 Vrms (±1 V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μV rms for the MF56CJ and 250 μV rms for the MF56-100. For ±2.5 V supplies the dynamic range is referenced to ±36 Vrms (±1.5 V peak) where the wideband noise over a 20 kHz bandwidth is typically 400 μV rms for both the MF56-50 and MF56-100.

**Note 3:** The specifications for the MF56 have been given for a clock frequency ($f_{CLK}$) of 250 kHz and above. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±1.25%, but the filter still maintains its magnitude characteristics. See Application Hints, Section 5.5.

**Note 4:** Besides checking the cutoff frequency ($f_c$) and the stopband attenuation at 2 $f_c$, additional functions are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB.

**Note 5:** For simplicity all the logic levels have been referenced to $V^* = 0$ V and will scale accordingly for ±5 V and ±2.5 V supplies (except for the TTL input logic levels).

**Note 6:** The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst-case conditions.

**Note 7:** The MF6 is operating with symmetrical split supplies and L Sh is tied to ground.

**Note 8:** Typical are at 25°C and represent most likely parametric norm.

**Note 9:** Test limits are guaranteed to National's ACOIL (Average Outgoing Quality Level).

**Note 10:** Design limits are guaranteed, but not 100% tested. These limits are not used to calculate outgoing quality levels.

**Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified conditions.

**Note 12:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

**Note 13:** When the input voltage ($V_{IN}$) at any pin exceeds the power supply rails ($V_{OH}$ or $V_{OL}$), the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.
Typical Performance Characteristics

**Schmitt Trigger Threshold Voltage vs Power Supply Voltage**

- Test voltages: V + = 15V, V - = 0V
- Temperature: Tj = 25°C

**Crosstalk from Filter to Op-Amps (MF6-100)**

- Test conditions:
  - V + = 10V
  - V - = 0V
  - Temperature: Tj = 25°C

**Crosstalk from Either Op-Amp to Filter Output (MF6-50)**

- Test conditions:
  - Temperature: Tj = 25°C
  - V + = 10V
  - V - = 0V

**Crosstalk from Filter to Op-Amps (MF6-50)**

- Test conditions:
  - Temperature: Tj = 25°C
  - V + = 10V
  - V - = 0V

**Equivalent Input Noise Voltage of Op-Amps**

- Test conditions:
  - Frequency: 1kHz
  - Temperature: Tj = 25°C
  - V + = 10V
  - V - = 0V

---

Gain of the filter:

- Gain is typically 200 µV/mV for wideband noise over a 20 dB
- The cutoff frequency begins to Section 1.5
- The magnitude response of
- Except for the TTL input logic
- And then shorting that output to voltage swing and then shorting

---

Notes:

- Current at that pin should be limited 5 mA current limit to four
- Ambient temperature, Tj. The ambient temperature, Tj, is lower
- J/W. For the MF6CU this number

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1-139
Typical Performance Characteristics (Continued)

**Positive Voltage Swing vs Power Supply Voltage**
- **Op Amp Output**
- **Filter Output**

**Positive Voltage Swing vs Power Supply Voltage**
- **Temperature (Filter and Op Amp Outputs)**

**Negative Voltage Swing vs Power Supply Voltage**
- **Filter and Op Amp Outputs**

**Power Supply Current vs Temperature**
- **Power Supply Voltage**

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TL140/5065-25
Typical Performance Characteristics (Continued)

- **f<sub>CLK</sub>/f<sub>B</sub> Deviation vs Clock Frequency**
- **f<sub>CLK</sub>/f<sub>B</sub> Deviation vs Temperature**
- **f<sub>CLK</sub>/f<sub>B</sub> Deviation vs Power Supply Voltage**
- **DC Gain Deviation vs Temperature**
- **DC Gain Deviation vs Power Supply Voltage**
- **DC Gain Deviation vs Clock Frequency**
Crosstalk Test Circuits

From Filter to Opamps

From Either Opamp to Filter Output

Pin Descriptions (Pin Numbers)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FILTER OUT (3)</td>
<td>The output of the lowpass filter. It will typically sink 0.9 mA and source 3 mA and swing to within 1V of each supply rail.</td>
<td>VOS (2)</td>
<td>VOS is the output, INV2 is the inverting input, and NINV2 is the non-inverting input of Op-Amp #1.</td>
</tr>
<tr>
<td>FILTER IN (8)</td>
<td>The input to the lowpass filter. To minimize gain errors the source impedance that drives this input should be less than 2k (see section 1.4). For single supply operation the input signal must be biased to mid-supply or AC coupled.</td>
<td>INV2 (14), NINV2 (1)</td>
<td>The positive and negative supply pins. The total power supply range is 5V to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.</td>
</tr>
<tr>
<td>VOSADJ (7)</td>
<td>This pin is used to adjust the DC offset of the filter output; it is not used it must be tied to the AGND potential. (See section 1.3)</td>
<td>V^+ (6), V^- (10)</td>
<td>A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self-clocking Schmitt-trigger oscillator (see section 1.1).</td>
</tr>
<tr>
<td>AGND (5)</td>
<td>The analog ground pin. This pin sets the DC bias level for the filter section and the non-inverting input of Op-Amp #1 and must be tied to the system ground for split supply operation or to mid supply for single supply operation (see section 1.2). When tied to mid-supply this pin should be well bypassed.</td>
<td>CLK IN (9)</td>
<td>A TTL logic level clock input when in split supply operation (±2.5V to ±7V) and L. Sh tied to system ground. This pin becomes a low impedance output when L. Sh is tied to V^- . Also used in conjunction with the CLK IN pin for a self-clocking Schmitt-trigger oscillator (see section 1.1).</td>
</tr>
<tr>
<td>VOS (4), INV1 (13)</td>
<td>VOS is the output and INV1 is the inverting input of Op-Amp #1. The non-inverting input of this Op-Amp is internally connected to the AGND pin.</td>
<td>CLK R (11)</td>
<td>Level shift pin, selects the logic threshold levels for the desired clock. When tied to V^- it enables an internal tri-state buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output.</td>
</tr>
</tbody>
</table>

1-142
1.0 MF6 Application Hints

The MF6 is comprised of a non-inverting unity gain lowpass sixth order Butterworth switched capacitor filter section and two undedicated CMOS Op-Amps. The switched capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the lowpass filter. Internal integrator time constants set the filter’s cutoff frequency. The resistive element of these integrators is actually a capacitor which is “switched” at the clock frequency (for a detailed discussion see Input Impedance Section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock to cutoff frequency ratio ($f_{CLK}/f_0$) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock to cutoff frequency ratio (or the sampling rate) the closer this approximation is to the theoretical Butterworth response. The MF6 is available in $f_{CLK}/f_0$ ratios of 50:1 (MF6-50) or 100:1 (MF6-100).

1.1 CLOCK INPUTS

The MF6 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. The oscillator’s frequency is dependent on the buffer’s threshold levels as well as on the resistor/capacitor tolerance (see Figure 1).

![Schmitt Trigger R/C Oscillator](image1)

**FIGURE 1. Schmitt Trigger R/C Oscillator**

![Dual Supply Operation](image2)

**FIGURE 2. Dual Supply Operation**

MF6 Driven with CMOS Logic Level Clock
($V_{IH} = 0.8 V_{CC}$ and $V_{IL} = 0.2 V_{CC}$ where $V_{CC} = V^- - V^+$)

![Dual Supply Operation](image3)

**FIGURE 3. Dual Supply Operation**

MF6 Driven with TTL Logic Level Clock
Application Hints (Continued)

a) Resistor Biasing of AGND

b) Using Op-Amp 2 to Buffer AGND

FIGURE 4. Single Supply Operation
Application Hints (Continued)

Schmitt-trigger threshold voltage levels can change significantly, causing the V/I oscillator's frequency to vary greatly from part to part. Where accuracy in f₂ is required an external clock can be used to drive the CLK R input of the MF6. This input is TTL logic level compatible and also presents a very light load to the external clock source (~2 µA) with split supplies and L Sh tied to system ground. The logic level is programmed by the voltage applied to level shift (L Sh) pin (See the Pin description for L Sh pin).

1.2 POWER SUPPLY BIASING

The MF6 can be biased from a single supply or dual split supplies. The split supply mode shown in Figures 2 and 3 is the most flexible and easiest to implement. As discussed earlier split supplies, ±5V to ±7V, will enable the use of TTL or CMOS clock logic levels. Figure 4 shows two schemes for single supply biasing. In this mode only CMOS clock logic levels can be used.

1.3 OFFSET ADJUST

The VosADJ pin is used in adjusting the output offset level of the filter section. If this pin is not used it must be tied to the analog ground (AGND) level, either mid-supply for single ended supply operation or ground for split supply operation. This pin sets the zero reference for the output of the filter. The implementation of this pin can be seen in Figure 5. In 5(a), DC offset is adjusted using a potentiometer; in 5(b), the Op-Amp integrator circuit keeps the average DC output level at AGND. The circuit in 5(b) is therefore appropriate only for AC-coupled signals and signals biased at AGND.

1.4 INPUT IMPEDANCE

The MF6 lowpass filter input (FILTER IN pin) is not a high impedance buffer input. This input is a switched capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the input to the filter can be seen in Figure 6. The input capacitor charges to the input voltage (V₂) during one half of the clock period, during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore Q = C₀V₂, and since current is defined as the flow of charge per unit time the average input current becomes

\[ Iₙ = \frac{Q}{T} \]

(where T equals one clock period) or

\[ Iₙ = \frac{C₀V₂}{T} = \frac{C₀V₂}{T_{CLK}} \]

The equivalent input resistor (Rₑ) then can be defined as

\[ Rₑ = \frac{V₂}{Iₙ} = \frac{1}{C₀T_{CLK}} \]

The input capacitor is 2 pF for the MF6-50 and 1 pF for the
Application Hints (Continued)

MF6-100, so for the MF6-100

\[ R_n = \frac{1 \times 10^{-12}}{f_{CLK}} - \frac{1 \times 10^{-12}}{f_C \times 100} - \frac{1 \times 10^{-10}}{f_C} \]

and

\[ R_n = \frac{5 \times 10^{11}}{f_{CLK}} - \frac{5 \times 10^{11}}{f_C \times 50} - \frac{1 \times 10^{10}}{f_C} \]

for the MF6-50. As shown in the above equations for a given cutoff frequency \( f_C \) the input impedance remains the same for the MF6-50 and the MF6-100. The higher the clock to center frequency ratio, the greater equivalent input resistance for a given clock frequency. As the cutoff frequency increases the equivalent input impedance decreases. This input resistance will form a voltage divider with the source impedance \( R_{source} \). Since, \( R_n \), is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain to the output of the filter. Since the filter's ideal gain is unity its overall gain is given by:

\[ A_V = \frac{R_n}{R_n + R_{source}} \]

If the MF6-50 or the MF6-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

\[ R_n = \frac{1 \times 10^{-10}}{10 \text{ kHz}} = 1 \text{ MΩ} \]

In this example with a source impedance of 10k the overall gain, if the MF6 had an ideal gain of 1 or 0 dB, would be:

\[ A_V = \frac{1 \text{ MΩ}}{10 \text{ kΩ} + 1 \text{ MΩ}} = 0.99909 \text{ or } -66.4 \text{ dB} \]

Since the maximum overall gain error for the MF6 is ±0.3 dB with a \( R_n \leq 2 \text{ kΩ} \) the actual gain error for this case would be +0.21 dB to −0.39 dB.

1.5 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency \( f_C \) has a lower limit caused by leakage currents through the internal switches discharging the stored charge on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

\[ f_{CLK} = 100 \text{ Hz}, \quad f_{leakage} = 1 \text{ pA}, \quad C = 1 \text{ pF} \]

\[ V = \frac{1 \text{ pA}}{1 \text{ pF} (100 \text{ Hz})} = 10 \text{ mV} \]

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors increases as the MF6 power supply voltage decreases. This causes a shift in the \( f_{CLK}/f_C \) ratio which will become noticeable when the clock frequency exceeds 250 kHz. The amplitude characteristic will stay within tolerance until \( f_{CLK} \) exceeds 500 kHz and will peak at about 0.5 dB at the corner frequency with a 1 MHz clock. The response of the MF6 is still a reasonable approximation of the ideal Butterworth lowpass characteristic as can be seen in Figure 7.

2.0 Designing with the MF6

Given any lowpass filter specification two equations will come in handy in trying to determine whether the MF6 can do the job. The first equation determines the order of the lowpass filter required:

\[ n = \frac{\log(10^{0.1} A_{min} - 1) - \log(10^{0.1} A_{max} - 1)}{2 \log(f_{C}/f_{CLK})} \]  \hspace{1cm} (1)

\[ A_{max} \text{ amplitude (dB)} \]

\[ A_{min} \text{ amplitude (dB)} \]

\[ f_{C} \text{ frequency (Hz)} \]

\[ f_{CLK} \text{ frequency (Hz)} \]

\[ 2 \text{ A 1 Suppo Amin} \]

\[ \text{This r quite} \]

\[ F \text{ Spe Muf} \]

\[ \text{Since the M MF6 2 with} \]

\[ \text{Attn where} \]

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\[ \text{F Spe Muf} \]

\[ \text{Since the M MF6 2 with} \]

\[ \text{Attn where} \]
Describing with the MF6 (Continued)

where \( n \) is the order of the filter, \( A_{\text{max}} \) is the minimum stopband attenuation (in dB) desired at frequency \( f_2 \), and \( A_{\text{max}} \) is the passband ripple or attenuation (in dB) at frequency \( f_2 \). If the result of this equation is greater than 6, then more than a single MF6 is required.

The attenuation at any frequency can be found by the following equation:

\[
A(f) = 10 \log \left( 1 + \left( \frac{10^{0.1A_{\text{max}}}}{10^{0.1f_2/n}} \right) \right) \text{ (dB)}
\]

where \( n = 6 \) (the order of the filter).

2.1 LOWPASS DESIGN EXAMPLE

Suppose the amplitude response specification in Figure 8 is given. Can the MF6 be used? The order of the Butterworth approximation will have to be determined using eq. 1:

\[
A_{\text{max}} = 30 \text{ dB}, \quad f_2 = 2 \text{ kHz}, \quad f_3 = 1 \text{ kHz}
\]

\[
n = \frac{\log(10^{f_2} - 1) - \log(10^{0.1})}{2 \log(2)} = 5.96
\]

Since \( n \) can only take on integer values, \( n = 6 \). Therefore the MF6 can be used. In general, if \( n \) is 6 or less a single MF6 stage can be utilized.

Likewise, the attenuation at \( f_2 \) can be found using equation 2 with the above values and \( n = 6 \) giving:

\[
A(f_2) = 10 \log \left( 1 + \left( \frac{10^{0.1A_{\text{max}}}}{10^{0.1f_2/n}} \right) \right) = 30.28 \text{ dB}
\]

This result also meets the design specification given in Figure 8, again verifying that a single MF6 section will be adequate.

![Figure 8. Design Example Magnitude Response Specification Where the Response of the Filter Design Must Fall Within the Shaded Area of the Specification](image)

To implement this example for the MF6-50 the clock frequency will have to be set to \( f_{\text{CLK}} = 50(1.116 \text{ kHz}) = 55.8 \text{ kHz} \) or for the MF6-100 \( f_{\text{CLK}} = 100(1.116 \text{ kHz}) = 111.6 \text{ kHz} \).

2.2 CASCADE MF6s

In the case where a steeper stopband attenuation rate is required two MF6's can be cascaded (Figure 9) yielding a 12th order slope of 72 dB per octave. Because the MF6 is a Butterworth filter and therefore has no ripple in its passband, when MF6s are cascaded the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1 V/V. The resulting response is shown in Figure 10.

In determining whether the cascaded MF6s will yield a filter that will meet a particular amplitude response specification, as above, equations 3 and 4 can be used, shown below.

\[
n = \frac{\log(10^{0.05A_{\text{max}}}) - \log(10^{0.05A_{\text{max}}})}{2 \log(10^{f_2})}
\]

\[
A(f) = 10 \log \left( 1 + \left( \frac{10^{0.05A_{\text{max}}}}{10^{0.05f_2/n}} \right) \right) \text{ (dB)}
\]

where \( n = 6 \) (the order of each filter). The attenuation \( A(f) \) will determine whether the order of the filter is adequate \((n \leq 6)\) while equation 4 can determine if the required stopband attenuation is met and what actual cutoff frequency \( f_3 \) is required to obtain the particular frequency response desired. The design procedure would be identical to the one shown in section 2.1.

2.3 IMPLEMENTING A "NOTCH" FILTER WITH THE MF6

A "notch" filter with 60 dB of attenuation can be obtained by using one of the Op-Amps, available in the MF6, and three external resistors. The circuit and amplitude response are shown in Figure 11.

The frequency where the "notch" will occur is equal to the frequency at which the output signal of the MF6 will have the same magnitude but be 180 degrees out of phase with its input signal. For a sixth order Butterworth filter 180° phase shift occurs where \( f = f_0 = 0.742 f_3 \). The attenuation at this frequency is 0.12 dB which must be compensated for by making \( R_1 = 1.014 \times R_2 \).

Since \( R_1 \) does not equal \( R_2 \) there will be a gain inequality above and below the notch frequency. At frequencies below the notch frequency \((f < f_0)\) the signal through the filter gains a one and is non-inverting. Summing this with the input signal through the Op-Amp yields an overall gain of two or +6 dB. For \( f > f_0 \) the signal at the output of the filter is greatly attenuated thus only the input signal will appear at the output of the Op-Amp. With \( R_3 = R_1 = 1.014 \) \( R_2 \) the overall gain is 0.986 or -0.12 dB at frequencies above the notch.
Designing with the MF6 (Continued)

Figure 9. Cascading Two MF6s

Figure 10a. One MF6-50 vs. Two MF6-50s Cascaded

Figure 10b. Phase Response of Two Cascaded MF6-50s
Designing with the MF6 (Continued)

![Circuit Diagram]

**FIGURE 11a. "Notch" Filter**

![Graph of Notch Filter Amplitude Response]

- $f_{ab} = 50$ kHz
- $V_{cc} = V^+ = V^- = 10V$

RE 10b. Phase Response of two Cascaded MF6-50s

FIGURE 11b. MF6-50 "Notch" Filter Amplitude Response
Designing with the MF6 (Continued)

2.4 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The MF6 will respond favorably to a sudden change in clock frequency. Distortion in the output signal occurs at the transition of the clock frequency and lasts approximately three cutoff frequency (f_c) cycles. As shown in Figure 12, if the control signal is low the MF6-50 has a 100 kHz clock making f_c = 2 kHz; when this signal goes high the clock frequency changes to 50 kHz yielding 1 kHz f_c.

The transient response of the MF6 seen in Figure 13 is also dependent on the f_c and thus the fCLK applied to the filter. The MF6 responds as a classical sixth order Butterworth lowpass filter.

![Image of transient response](TL/H/5065-30)

**FIGURE 12. MF6-50 Abrupt Clock Frequency Change**

2.5 ALIASING CONSIDERATIONS

Aliasing effects have to be taken into consideration when input signal frequencies exceed half the sampling rate. For the MF6 this equals half the clock frequency (fCLK). When

![Input Signal Spectrum](TL/H/5065-37)

(a) Input Signal Spectrum

![Output Signal Spectrum](TL/H/5065-38)

(b) Output Signal Spectrum. Note that the input signal at f_s/2 + f raises an output signal to appear at f_s/2 - f.

Figure 14. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the MF6, f_s = fCLK.
Designing with the MF6 (Continued)

Input Response, Vertical = 1 ms/div., $f_{CLK} = 100$ kHz component at a frequency higher than the Nyquist rate, as in Figure 14e, that component is aliased into the frequency band $f_{CLK}/2$. If this component is a filter, and of large enough amplitude, it can be difficult to remove. Therefore, if frequency components $f_{CLK}/2$ and $2f_{CLK}$ are to be attenuated, they must be attenuated in the MF6 input. The necessary attenuation varies depending on system requirements. For system requirements, the signal component is attenuated at least to the 8th order, or a higher order. An example circuit is shown in Figure 15, with an uncommitted Op-Amp available.

\[
I_0 = \frac{1}{2 - e^{R_1 R_2 - R_2}}
\]

$H_0 = R_4/R_2$ (If $P_0 = 1$, then $R_3$ and $R_4$ are omitted and $Y_{C2}$ is directly tied to INV2).

**Design Procedure:**

1. peak $C_1$ for a 2nd Order Butterworth
2. $Q = 0.707$
3. $R_2 = \frac{1}{2Q_{v2}}$
4. $C_1 = \frac{1}{2Q_{v2}}$
5. $R_2 = \frac{C_1}{2}$
6. $R_1 = R_2$
7. $C_2 = \frac{1}{2R_2 R_1 C_1}$

Note: The parallel combination of $R_2$ (if used), $R_1$, and $R_2$ should be > 10 kΩ in order not to load Op-Amp #2.

**FIGURE 15.** Second Order Butterworth Anti-Aliasing Filter Using Uncommitted Op-Amp #2