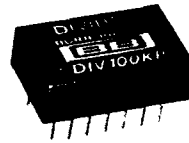




**DIV100**



## ANALOG DIVIDER

### FEATURES

- **HIGH ACCURACY**  
0.25% maximum error, 40:1 denominator range
- **TWO-QUADRANT OPERATION**  
Dedicated log-antilog technique
- **EASY TO USE**  
Laser-trimmed to specified accuracy - no external resistors needed
- **LOW COST**
- **DIP PACKAGE**

### APPLICATIONS

- **DIVISION**
- **SQUARE ROOT**
- **RATIOMETRIC MEASUREMENT**
- **PERCENTAGE COMPUTATION**
- **TRANSDUCER AND BRIDGE LINEARIZATION**
- **AUTOMATIC LEVEL - AND GAIN - CONTROL**
- **VOLTAGE CONTROLLED AMPLIFIERS**
- **ANALOG SIMULATION**

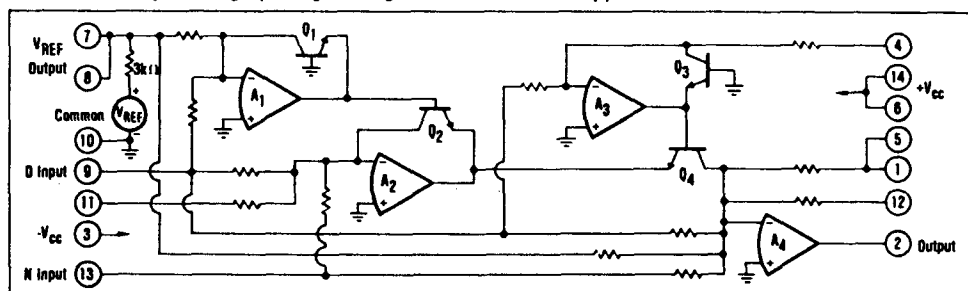
### DESCRIPTION

The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and logging transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment - the DIV100 is a complete, single package analog divider.

For those applications requiring higher accuracy than the DIV100 specifies the capability for optional adjustment is provided. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error.

The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BURCORP - Telex: 66-6491

PDS-427A

# SPECIFICATIONS

## ELECTRICAL

Specifications at  $T_A = +25^\circ\text{C}$  and  $\pm V_{CC} = 15\text{VDC}$  unless otherwise noted.

MODEL	PARAMETER	CONDITIONS	DIV100HP			DIV100JP			DIV100KP			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSFER FUNCTION			$V_O = 10N/D$									
ACCURACY			$R_L \geq 10k\Omega$									
Total Error												
Initial		$0.25V \leq D \leq 10V, N \leq  D $		0.7	1.0		0.3	0.5		0.2	0.25	% FSO(1)
vs. Temperature		$1V \leq D \leq 10V, N \leq  D $		0.02	0.05(2)		*	*		*	*	% FSO/°C
vs. Supply		$0.25V \leq D \leq 1V, N \leq  D $		0.08	0.2(2)		*	*		*	*	% FSO/°C
Warm-up time to rated performance		$0.25V \leq D \leq 10V, N \leq  D $		0.15			*	*		*	*	% FSO/%
				5			*	*		*	*	Minutes
AC PERFORMANCE			$D = +10V$									
Small-Signal Bandwidth		-3dB		350		*	*	*	*	*	*	kHz
0.5% Amplitude Error		Small-Signal		15		*	*	*	*	*	*	kHz
0.57° Vector Error		Small-Signal		1000		*	*	*	*	*	*	Hz
Full-Power Bandwidth		$V_O = \pm 10V, I_O = \pm 5mA$		30		*	*	*	*	*	*	kHz
Slew Rate		$V_D = \pm 10V, I_O = \pm 5mA$		2		*	*	*	*	*	*	V/ $\mu\text{sec}$
Settling Time		$\epsilon = 1\%, \Delta V_O = 20V$		15		*	*	*	*	*	*	$\mu\text{sec}$
Overload Recovery		50% Output Overload		4		*	*	*	*	*	*	$\mu\text{sec}$
INPUT CHARACTERISTICS												
Input Voltage Range												V
Numerator		$N \leq  D $		$\pm 10$		*	*	*	*	*	*	V
Denominator		$D \geq +250mV$		+10		*	*	*	*	*	*	V
Input Resistance		Either Input		25		*	*	*	*	*	*	k $\Omega$
OUTPUT CHARACTERISTICS												
Full-Scale Output (FSO)				$\pm 10$		*	*	*	*	*	*	V
Rated Output						*	*	*	*	*	*	V
Voltage		$I_O = \pm 5mA$		$\pm 10$		*	*	*	*	*	*	V
Current		$V_O = \pm 10V$		$\pm 5$		*	*	*	*	*	*	mA
Current Limit						*	*	*	*	*	*	mA
Positive				15	20(2)	*	*	*	*	*	*	mA
Negative				19	23(2)	*	*	*	*	*	*	mA
OUTPUT NOISE VOLTAGE			$N = 0V$									
$f_B = 10\text{Hz to } 10\text{kHz}$												$\mu\text{V, rms}$
$D = +10V$				370		*	*	*	*	*	*	mV, rms
$D = +250mV$				1		*	*	*	*	*	*	
REFERENCE VOLTAGE CHARACTERISTICS			$R_L \geq 10M\Omega$									
Output Voltage												V
Initial		At $+25^\circ\text{C}$		6.3(2)	6.6	6.9(2)	*	*	*	*	*	$\mu\text{V/V}$
vs. Supply				$\pm 25$		*	*	*	*	*	*	ppm/°C
Temperature Coefficient				$\pm 50$		*	*	*	*	*	*	ppm/°C
Output Resistance				3		*	*	*	*	*	*	k $\Omega$
POWER SUPPLY REQUIREMENTS												
Rated Voltage												VDC
Operating Range		Derated Performance		$\pm 12$	$\pm 15$	$\pm 20$	*	*	*	*	*	VDC
Quiescent Current							*	*	*	*	*	mA
Positive Supply				5	7(2)		*	*	*	*	*	mA
Negative Supply				8	10(2)		*	*	*	*	*	mA
AMBIENT TEMPERATURE RANGE												
Specification				0	+70	*	*	*	*	*	*	°C
Operating Range		Derated Performance		-25	+85	*	*	*	*	*	*	°C
Storage				-40	+86	*	*	*	*	*	*	°C

\*Same as DIV100HP.

NOTES: (1) FSO is the abbreviation for Full Scale Output. (2) This parameter is untested and is not guaranteed. This specification is established to a 90% confidence level. (3) See General Information section for discussion. (4) For supply voltages less than  $\pm 20\text{VDC}$ , the absolute maximum input voltage is equal to the supply voltage. (5) Short-circuit may be to ground only. Rating applies to an ambient temperature of  $+38^\circ\text{C}$  at rated supply voltage.

### ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 20\text{VDC}$
Internal Power Dissipation <sup>(1)</sup>	600mW
Input Voltage Range <sup>(2)</sup>	$\pm 20\text{VDC}$
Storage Temperature Range	$-55^\circ\text{C to } +125^\circ\text{C}$
Operating Temperature Range	$-25^\circ\text{C to } +85^\circ\text{C}$
Lead Temperature (soldering, 10 seconds)	$+300^\circ\text{C}$
Output Short-Circuit Duration <sup>(3)</sup>	Continuous
Junction Temperature	$+175^\circ\text{C}$

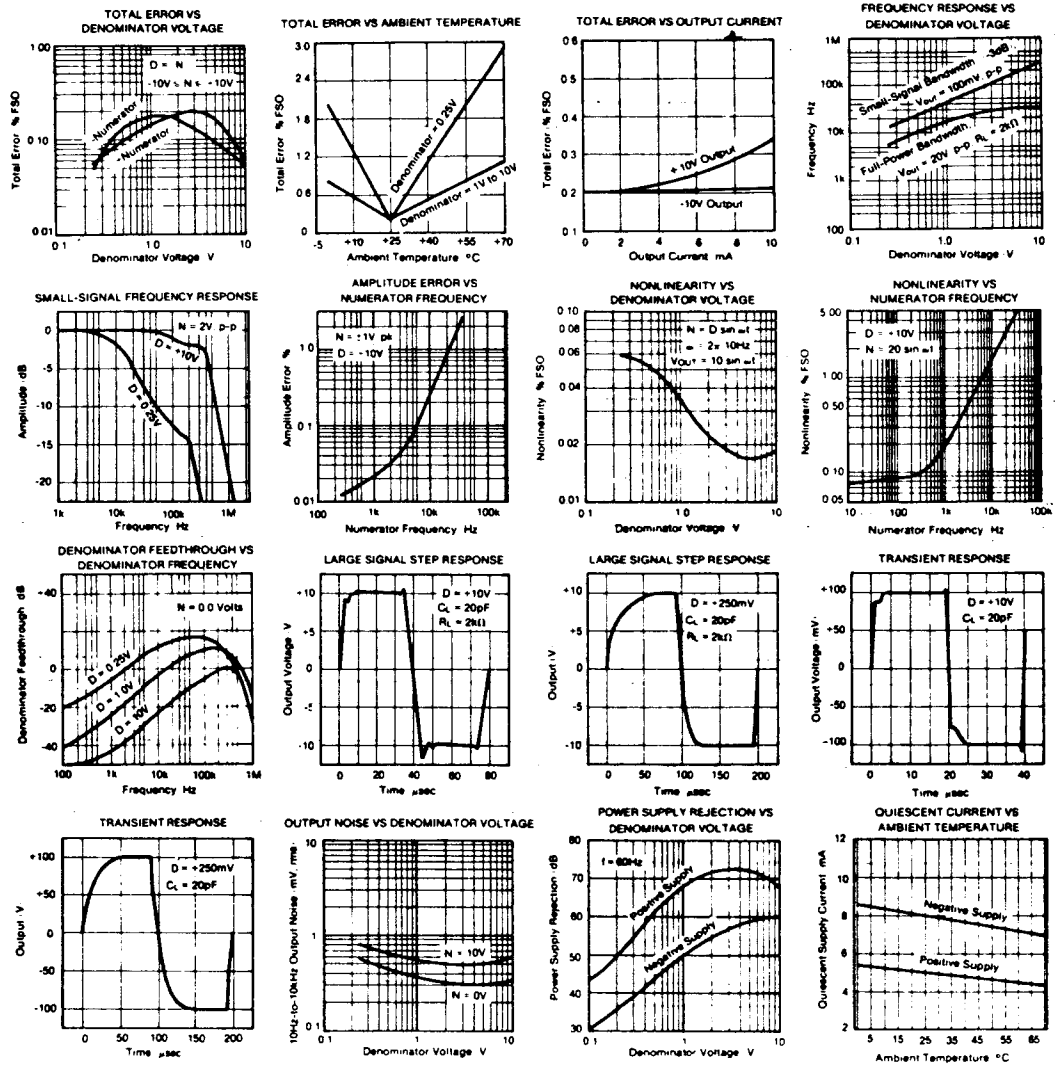
DIV100

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ANALOG CIRCUIT FUNCTIONS

# TYPICAL PERFORMANCE CURVES

T<sub>A</sub> = +25°C, V<sub>CC</sub> = ±15VDC unless otherwise noted



## PIN CONFIGURATION

1. Gain Error Adjust  
 2. Output  
 3. -V<sub>CC</sub>  
 4. D Input Offset Adjust  
 5. Internally Connected to Pin 1  
 6. Internally Connected to Pin 14  
 7. Internally Connected to Pin 8  
 8. Reference Voltage  
 9. Denominator (D) Input  
 10. Common  
 11. N Input Offset Adjust  
 12. Output Offset Adjust  
 13. Numerator (N) Input  
 14. +V<sub>CC</sub>

Bottom View

○14	1 ○
○13	2 ○
○12	3 ○
○11	4 ○
○10	5 ( )
○9	6 ○
○8	7 ○

## MECHANICAL

ORDER NUMBER: { DIV100HP  
 DIV100JP  
 DIV100KP

CASE Epoxy  
 WEIGHT 27 Grams  
 CONNECTOR 0145MC

NOTE:  
 Leads in true position within  
 0.010" ± 0.25mm R at MMC at  
 seating plane  
 Denotes Pin 1

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.780	.810	20.07	20.57
B	.490	.510	12.45	12.95
C	.190	.260	4.83	6.60
D	.018	.021	0.46	0.53
G	1.00 BASIC		2.54 BASIC	
H	.080	.118	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.118	2.03	2.92

Pin numbers shown for reference only. Numbers are not marked on package.

## DEFINITIONS

### TRANSFER FUNCTION

The ideal transfer function for the DIV100 is:

$$V_{out} = 10 \frac{N}{D}$$

where: N = Numerator input voltage  
D = Denominator input voltage  
10 = Internal scale factor

Figure 1 shows the operating region over the specified numerator and denominator ranges. Note that below the minimum denominator voltage (250mV) operation is undefined.

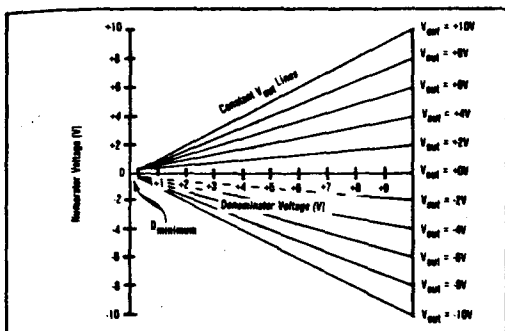


FIGURE 1. Operating Region.

### ACCURACY

Accuracy is specified as a percentage of full-scale output (FSO). It is derived from the total error specification.

### TOTAL ERROR

Total error is the deviation of the actual output from the ideal quotient  $10 \frac{N}{D}$  expressed in percent of FSO (10V); e.g., for the DIV100K:

$$V_{out \text{ actual}} = V_{out \text{ ideal}} \pm \text{total error,}$$

where: Total error = 0.25% FSO = 25mV.

It represents the sum of all error terms normally associated with a divider: numerator nonlinearity, denominator nonlinearity, scale-factor error, output-referred numerator and denominator offsets, and the offset due to the

output amplifier. Individual errors are not specified because it is their sum that affects the user's application.

### SMALL-SIGNAL BANDWIDTH

Small-signal bandwidth is the frequency the output drops to 70% (-3dB) of its DC value. The input signal must be low enough in amplitude to keep the divider's output from becoming slew-rate limited. A rule-of-thumb is to make the output voltage 100mV, p-p, when testing this parameter. Small-signal bandwidth is directly proportional to denominator magnitude as described in the Typical Performance Curves.

### 0.5% AMPLITUDE ERROR

At high frequencies the input-to-output relationship is a complex function that produces both a magnitude and vector error. The 0.5% amplitude error is the frequency at which the magnitude of the output drops 0.5% from its DC value.

### 0.57° VECTOR ERROR

The 0.57° vector error is the frequency at which a phase error of 0.01 radians occurs. This is the most sensitive measure of dynamic error of a divider.

### LINEARITY

Defining linearity for a nonlinear device may seem unnecessary; however, by keeping one input constant the output becomes a linear function of the remaining input. The denominator is the input that is held fixed with a divider. Nonlinearities in a divider add harmonic distortion to the output in the amount of:

$$\text{Percent Distortion} \approx \frac{\text{Percent Nonlinearity}}{\sqrt{2}}$$

### FEEDTHROUGH

Feedthrough is the signal at the output for any value of denominator within its rated range, when the numerator input is zero. Ideally the output should be zero under this condition.

## GENERAL INFORMATION

### WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the +V<sub>CC</sub> and -V<sub>CC</sub> pins to the power supply common. The connection of these capacitors should be as close to the DIV100 as practical.

### CAPACITIVE LOADS

Stable operation is maintained with capacitive loads of up to 1000pF, typically. Higher capacitive loads can be driven if a 22Ω carbon resistor is connected in series with the DIV100's output.

### OVERLOAD PROTECTION

The DIV100 can be protected against accidental power supply reversal by putting a diode (1N4001, type) in series with each power supply line as shown in Figure 2. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off.

If this protection circuit is used, the accuracy of the DIV100 will be degraded by the power supply sensitivity specification. No other overload protection circuit is necessary. Inputs are internally protected against over-voltages and they are current-limited by at least a 10kΩ series resistor. The output is protected against short circuits to power supply common only.

DIV100

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ANALOG CIRCUIT FUNCTIONS

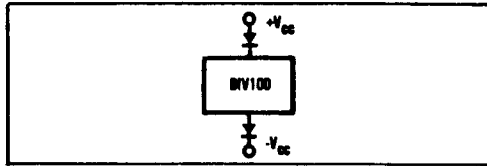


FIGURE 2. Overload Protection Circuit.

### STATIC SENSITIVITY

No special handling is required. The DIV100 does not use MOS-type transistors. Furthermore, all external leads are protected by resistors against low energy electrostatic discharge (ESD).

### INTERNAL POWER DISSIPATION

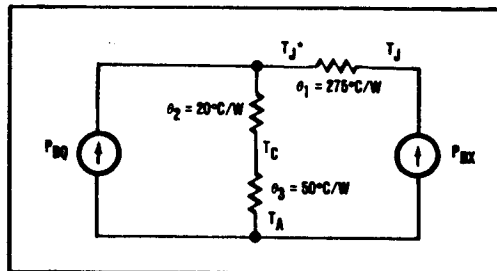


FIGURE 3. DIV100 Thermal Model.

Figure 3 is the thermal model for the DIV100 where:

$P_{DQ}$  = Quiescent Power Dissipation

$$= | +V_{CC} | I_{\text{QUIESCENT}} + | -V_{CC} | I_{\text{QUIESCENT}}$$

$P_{DX}$  = Worst case power dissipation in the output transistor

$$= V_{CC}^2 / 4R_{\text{LOAD}} \text{ (for normal operation)}$$

$$= V_{CC} I_{\text{output limit}} \text{ (for short-circuit)}$$

## THEORY OF OPERATION

The DIV100 is a log-antilog divider consisting of four operational amplifiers and four logging transistors integrated into a single monolithic circuit. Its basic principal of operation can be seen by an analysis of the circuit in Figure 4.

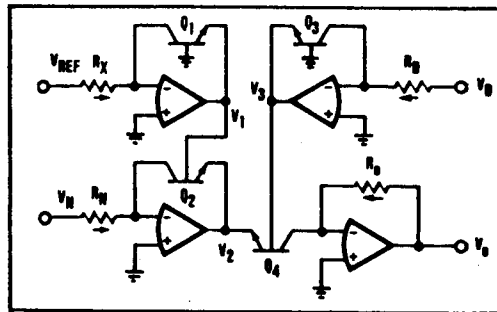


FIGURE 4. One-Quadrant Log-Antilog Divider.

The logarithmic equation for a bipolar transistor is:

$$V_{BE} = V_T \ln(I_c/I_s) \quad (1)$$

$T_J$  = Junction Temperature (output loaded)

$T_J^*$  = Junction Temperature (no load)

$T_C$  = Case Temperature

$T_A$  = Ambient Temperature

$\theta$  = Thermal Resistance

This model is obviously not the simple one power source model that most linear device manufacturers give. It is, however, a more accurate model for a multidevice monolithic or hybrid integrated circuit.

The model in Figure 3 must be used in conjunction with the DIV100's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem:

Determine the highest ambient temperature at which the DIV100 may be operated with a continuous short circuit to ground.  $V_{CC} = \pm 15\text{VDC}$ .

$$P_{D(\text{max})} = 600\text{mW}, T_{J(\text{max})} = +175^\circ\text{C}.$$

$$T_A = T_{J(\text{max})} - P_{DQ}(\theta_2 + \theta_3) - P_{DX(\text{short-circuit})}(\theta_1 + \theta_2 + \theta_3) \\ = 175^\circ\text{C} - 18^\circ\text{C} - 119^\circ\text{C} = 38^\circ\text{C}$$

$$P_{D(\text{actual})} = P_{DQ} + P_{DX(\text{short-circuit})} \leq P_{D(\text{max})} \\ = 255\text{mW} + 345\text{mW} = 600\text{mW}$$

The conclusion is that the device will withstand a short-circuit up to  $T_A = +38^\circ\text{C}$  without exceeding either the  $175^\circ\text{C}$  or  $600\text{mW}$  absolute maximum limits.

### LIMITING OUTPUT VOLTAGE SWING

The negative output voltage swing should be limited to  $\pm 11\text{V}$ , maximum, to prevent polarity inversion and possible system instability. This should be done by limiting the input voltage range.

where:  $V_T = kT/q$

$k$  = Boltzmann's constant =  $1.381 \times 10^{-23}$

$T$  = Absolute temperature in degrees Kelvin

$q$  = Electron charge =  $1.602 \times 10^{-19}$

$I_c$  = Collector current

$I_s$  = Reverse saturation current

Applying equation (1) to the four logging transistors gives:

For  $Q_1$ :

$$V_{BE} = V_B - V_E = V_T [\ln(V_{REF}/R_X) - \ln I_c]$$

This leads to:

$$V_1 = -V_T [\ln(V_{REF}/R_X) - \ln I_c]$$

For  $Q_2$ :

$$V_1 - V_2 = V_T [\ln(V_N/R_N) - \ln I_s]$$

For  $Q_3$ :

$$V_3 = -V_T [\ln(V_D/R_D) - \ln I_s]$$

We have now taken the logarithms of the input voltage  $V_{REF}$ ,  $V_N$ , and  $V_D$ . Applying equation (1) to  $Q_4$  gives:

$$V_3 - V_2 = V_T [\ln(V_o/R_o) - \ln I_c]$$

Assume  $V_T$  and  $I_s$  are the same for all four transistors (a reasonable assumption with a monolithic IC). Solving

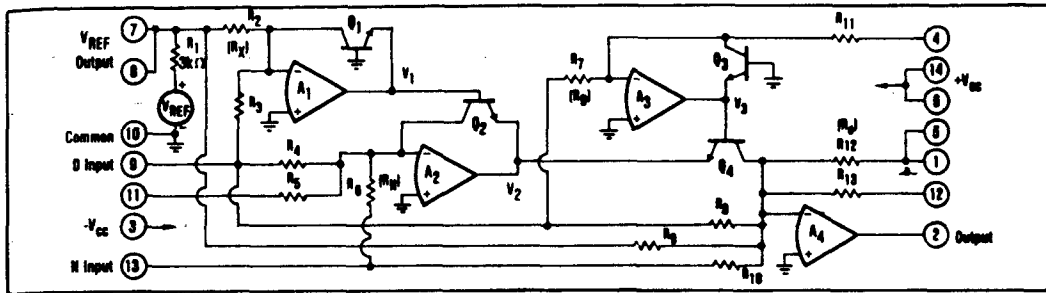


FIGURE 5. DIV100 Two-Quadrant Log-Antilog Circuit.

this last equation in terms of the previously defined variables and taking the antilogarithm of the result yields:

$$V_o = \frac{V_{REF} V_N R_o R_D}{V_D R_X R_N} \quad (2)$$

In the DIV100  $V_{REF} = 6.6V$ ,  $R_o = R_N = R_{10}$ , and  $R_X$  is such that the transfer function is:

$$V_o = 10 N D \quad (3)$$

where: N = Numerator Voltage  
D = Denominator Voltage

Figure 5 is a more detailed circuit diagram for the DIV100. In addition to the circuitry included in Figure 3, it also shows the resistors ( $R_3$ ,  $R_4$ ,  $R_5$ , and  $R_{10}$ ) used for level-shifting. This converts the DIV100 to a two-quadrant divider.

The implementation of the transfer function is equation (3) is done using devices with real limitations. For example, the value of the D input must always be positive. If it isn't,  $Q_3$  will no longer conduct,  $A_3$  will become open loop, and its output and the DIV100 output will saturate. This limitation is further restricted in that if the D input is less than +250mV the errors will become substantial. It will still function, but its accuracy will be less.

Still another limitation is the value of the N input must always be equal to or less than the absolute value of the D input. From equation (3) it can be seen that if this

limitation is not met  $V_o$  will try to be greater than the 10V output voltage limit of  $A_4$ .

A limitation that may not be obvious is the effect of source resistance. If the numerator or denominator inputs are driven from a source with more than 10Ω of output resistance, the resultant voltage divider will cause a significant output error. This voltage divider is formed by the source resistance and the DIV100 input resistance. With  $R_{SOURCE} = 10\Omega$  and  $R_{INPUT(DIV100)} = 25k\Omega$  an error of 0.04% results. This means that the best performance of the DIV100 is obtained by driving its inputs from operational amplifiers.

Note that the reference voltage is brought out to pins 7 and 8. This gives the user a precision, temperature-compensated reference for external use. Its open-circuit voltage is +6.6VDC,  $\pm 0.075V$ , typically. Its Thevenin equivalent resistance is 3kΩ. Since the output resistance is a relatively high value, an operational amplifier is necessary to buffer this source as shown in Figure 6. The external amplifier is necessary because current drawn through the 3kΩ resistor will effect the DIV100 scale factor.

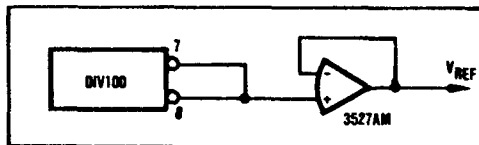


FIGURE 6. Buffered Precision Voltage Reference.

## OPTIONAL ADJUSTMENTS

Figure 7 shows the connections to make to adjust the DIV100 for significantly better accuracy over its 40-to-1 denominator range.

The adjustment procedure is:

1. Begin with  $R_1$ ,  $R_2$ , and  $R_3$  set to their mid-position.
2. With  $|N| = D = 10.000V$ ,  $\pm 1mV$ , adjust  $R_1$  for  $V_o = +10.000V$ ,  $\pm 1mV$ . This sets the scale factor.
3. Set D to the minimum expected denominator voltage. With  $N = -D$ , adjust  $R_2$  for  $V_o = -10.000V$ . This adjusts the output referred denominator offset errors.
4. With D still at its minimum expected value, make  $N = D$ . Adjust  $R_3$  for  $V_o = 10.000V$ . This adjusts the output referred offset errors.
5. Repeat steps 2-4 until the best accuracy is obtained.

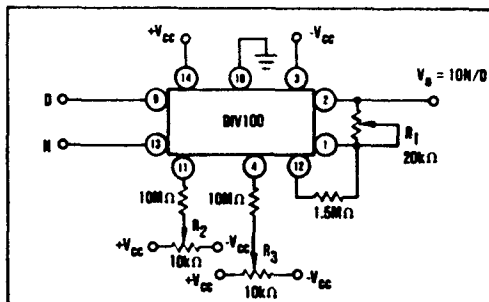


FIGURE 7. Connection Diagram for Optional Adjustments.



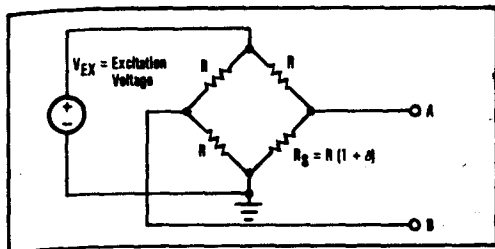


FIGURE 13. Bridge Circuit.

The differential output voltage  $V_{RA}$  is:

$$V_{RA} = V_H - V_A = \frac{-V_{EX}\delta}{2(2 + \delta)}$$

a nonlinear function of the resistance change in the active arm. This nonlinearity limits the useful span of the bridge to perhaps  $\pm 10\%$  variation in the measured parameter.

Bridge linearization is accomplished using the circuit in Figure 14. The instrumentation amplifier converts the differential output to a single-ended voltage needed to drive the divider. The voltage-divider string makes the numerator and denominator voltages:

$$N = \frac{-V_{EX}\delta R_{IN}}{(2R_1 + 3R_{IN})(2 + \delta)} \text{ , and ,}$$

$$D = \frac{2 V_{EX} R_{ID}}{(2R_1 + 3R_{ID})(2 + \delta)} \text{ , respectively ,}$$

where:  $R_{IN}$  = DIV100 numerator input resistance

$R_{ID}$  = DIV100 denominator input resistance

Applying these voltages to the DIV100 transfer function gives:

$$V_o = 10N D = \frac{(2R_1 + 3R_{ID})(R_{IN}\delta) 10}{(2R_1 + 3R_{IN})(2R_{ID})}$$

which reduces to:

$$V_o = -5\delta$$

if the divider's input resistances are equal.

The nonlinearity of the bridge has been eliminated and the circuit output is independent of variations in the excitation voltage.

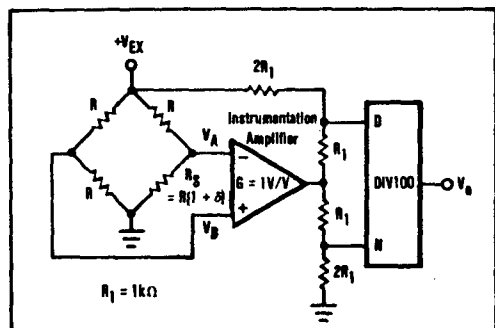


FIGURE 14. Bridge Linearization Circuit.

#### AUTOMATIC GAIN CONTROL

A simple AGC circuit using the DIV100 is shown in Figure 15. The numerator voltage may vary both positive and negative. The divider's output is half-wave rectified and filtered by  $D_1$ ,  $R_3$ , and  $C_2$ . It is then compared to the DC reference voltage. If a difference exists the integrator

sends a control signal to the denominator input to maintain a constant output, thus compensating for input voltage changes.

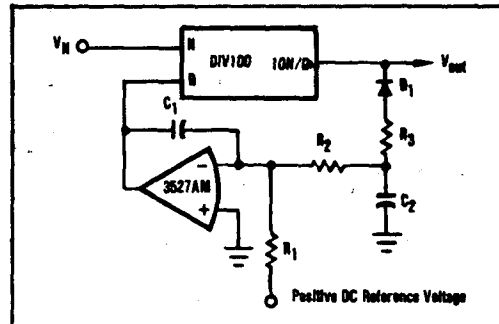


FIGURE 15. Automatic Gain Control Circuit.

#### VOLTAGE-CONTROLLED FILTER

Figure 16 shows how to use the DIV100 in the feedback loop of an integrator to form a voltage-controlled filter. The transfer function is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{K}{\tau s + 1}$$

where:  $K = -R_2/R_1$

$$\tau = \frac{10 R_2 C}{V_{CONTROL}}$$

This circuit may be used as a single-pole low-pass active filter whose cutoff frequency is linearly proportional to the circuit's control voltage.

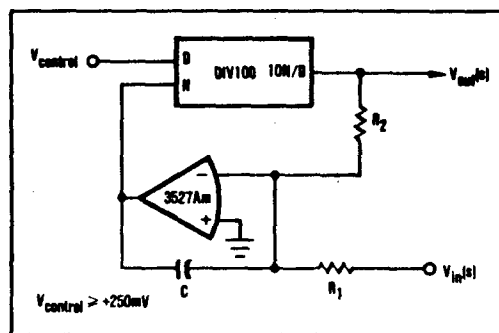


FIGURE 16. Voltage - Controlled Filter.

#### SQUARE ROOT

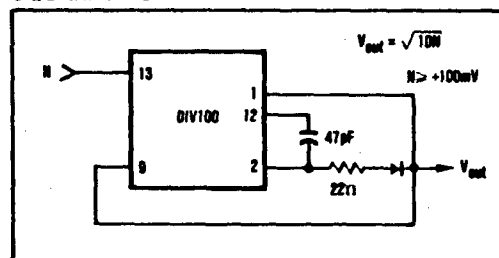


FIGURE 17. Connection Diagram for Square Root Mode.