MONOLITHIC FOUR-QUADRANT MULTIPLIER

... designed for use where the output voltage is a linear product of two input voltages. Typical applications include multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

The MC1594/1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power supply rejection.

- Operates With ±15 V Supplies
- Excellent Linearity – Maximum Error (X or Y): ± 0.5% (MC1594)
- ± 1.0% (MC1494)

- Wide Input Voltage Range ±10 volts
- Adjustable Scale Factor, K (0.1 nominal)
- Single Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small Signal) > 1.0 MHz
- Power Supply Sensitivity – 30 mV/V typical
### MC1494L, MC1594L

**MAXIMUM RATINGS** (TA = +25°C unless otherwise noted)

<table>
<thead>
<tr>
<th>Rating</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage</td>
<td>V+</td>
<td>+18</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td>V-</td>
<td>-18</td>
<td></td>
</tr>
<tr>
<td>Differential Input Signal</td>
<td>VBP-VB</td>
<td>≤±18</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td>VP-VP</td>
<td>≤±18</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Input Voltage</td>
<td>VCMX = V9 = V6</td>
<td>≤11.5</td>
<td>Vdc</td>
</tr>
<tr>
<td></td>
<td>VCMX</td>
<td>≤11.5</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation (Package Limitation)</td>
<td>PD</td>
<td>750</td>
<td>mW</td>
</tr>
<tr>
<td>Derate above T93 = +25°C</td>
<td>1/°C/KA</td>
<td>5.0</td>
<td>mW/°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>MC1594</td>
<td>TA</td>
<td>-55 to +125°C</td>
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<tr>
<td></td>
<td>MC1494</td>
<td></td>
<td>0 to +70°C</td>
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<tr>
<td>Storage Temperature Range</td>
<td>T93</td>
<td>-65 to +150°C</td>
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</table>

**ELECTRICAL CHARACTERISTICS** (V+ = +15 V, V- = -15 V, TA = +25°C, R1 = 16 kΩ, R1 = 30 kΩ, RY = 62 kΩ, RL = 47 kΩ, unless otherwise noted)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Fig.</th>
<th>Symbol</th>
<th>MC1594</th>
<th>MC1494</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
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<td>Linearity</td>
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<td>Error in Percent of full scale</td>
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<td>±0.5</td>
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<td>%</td>
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<tr>
<td>Output Voltage Range (VX = VY = VY)</td>
<td>2,3,4</td>
<td>Vin</td>
<td>±10</td>
<td>±10</td>
<td>±10</td>
<td>±Vpk</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>Resistance (X or Y Input)</td>
<td>R</td>
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<td>±100</td>
<td>±100</td>
<td>±100</td>
<td>±100</td>
<td>kΩ</td>
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<tr>
<td>Offset Voltage (X Input)</td>
<td>VOX</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>V</td>
<td></td>
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<tr>
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<td>±0.5</td>
<td>±0.5</td>
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<td>±0.5</td>
<td>V</td>
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<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>μA</td>
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<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>±0.5</td>
<td>nA</td>
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<td>±100</td>
<td>±100</td>
<td>±100</td>
<td>±100</td>
<td>kΩ</td>
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<td>VO</td>
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<td>±100</td>
<td>±100</td>
<td>±100</td>
<td>±100</td>
<td>V</td>
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<td>TA = Thigh to Tlow</td>
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<tr>
<td>Output Offset (X = 0, Y = 0)</td>
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<tr>
<td>Voltage Current</td>
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<td>±1.3</td>
<td>±1.3</td>
<td>±1.3</td>
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<td>X Input Offset (X = 0)</td>
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<td>±27</td>
<td>±27</td>
<td>±27</td>
<td>±27</td>
<td>nA/°C</td>
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<tr>
<td>Y Input Offset (X = 0)</td>
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<td>±1.5</td>
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<td>nA/°C</td>
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<td>±0.07</td>
<td>±0.07</td>
<td>±0.07</td>
<td>±0.07</td>
<td>%/°C</td>
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<td>±0.09</td>
<td>±0.09</td>
<td>±0.09</td>
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<td>%/°C</td>
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<td>±0.8</td>
<td>±0.8</td>
<td>±0.8</td>
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<td>2° Relative Phase Shift</td>
<td>Pp</td>
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<td>±40</td>
<td>±40</td>
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<td>±40</td>
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<td>1° Absolute Error</td>
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<td>±10.5</td>
<td>±10.5</td>
<td>±10.5</td>
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<td>Input Swing (X or Y)</td>
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<td>±65</td>
<td>±65</td>
<td>±65</td>
<td>±65</td>
<td>V</td>
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<tr>
<td>Gain (X or Y)</td>
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<tr>
<td>Sensitivity</td>
<td>S+</td>
<td>±1.3</td>
<td>±1.3</td>
<td>±1.3</td>
<td>±1.3</td>
<td>±1.3</td>
<td>mV/V</td>
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<td>Regulated Offset Adjust Voltages</td>
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<td>V(+)</td>
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<td>±3.5</td>
<td>±3.5</td>
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<td>±3.5</td>
<td>±3.5</td>
<td>±3.5</td>
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<tr>
<td></td>
<td>Negative</td>
<td>V(-)</td>
<td>±3.5</td>
<td>±3.5</td>
<td>±3.5</td>
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<td>±3.5</td>
<td>±3.5</td>
<td>±3.5</td>
<td>±3.5</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Offsets can be adjusted to zero with external potentiometers. Thigh = +125°C for MC1594, +70°C for MC1494, -50°C for MC1594, 0°C for MC1494.

**MOTOROLA LINEAR/INTERFACE DEVICES**

11-12
MC1494L, MC1594L

TEST CIRCUITS

FIGURE 1 - LINEARITY

FIGURE 2 - INPUT RESISTANCE

FIGURE 3 - OFFSET VOLTAGES, GAIN

FIGURE 4 - INPUT BIAS CURRENT/INPUT OFFSET CURRENT, OUTPUT RESISTANCE

FIGURE 5 - FREQUENCY RESPONSE

FIGURE 6 - COMMON MODE

FIGURE 7 - POWER-SUPPLY SENSITIVITY

FIGURE 8 - BURN-IN

MOTOROLA LINEAR/INTERFACE DEVICES

11-13
MC1494L, MC1594L

TYPICAL CHARACTERISTICS
(Unless otherwise noted, $V^+ = +15\,\text{V}$, $V^- = -15\,\text{V}$, $R1 = 16\,\text{k}\Omega$, $R_X = 30\,\text{k}\Omega$, $R_Y = 62\,\text{k}\Omega$, $R_L = 47\,\text{k}\Omega$, $T_A = +25^\circ\text{C}$)

**FIGURE 9** — FREQUENCY RESPONSE OF Y INPUT versus LOAD RESISTANCE

**FIGURE 10** — FREQUENCY RESPONSE OF X INPUT versus LOAD RESISTANCE

**FIGURE 11** — LARGE SIGNAL VOLTAGE versus FREQUENCY

**FIGURE 12** — LINEARITY versus $R_X$ OR $R_Y$ WITH $K = 1/10$

**FIGURE 13** — LINEARITY versus $R_X$ OR $R_Y$ WITH $K = 1$

**FIGURE 14** — SCALE FACTOR ($K$) versus TEMPERATURE

MOTOROLA LINEAR/INTERFACE DEVICES
11-14
MC1494L, MC1594L

CIRCUIT DESCRIPTION

Introduction
The MC1594 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a single-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltage.

As shown in Figure 15, the MC1594 consists of a multiplier proper and associated peripheral circuitry to provide these features.

GENERAL INFORMATION

FIGURE 15
(Recommended External Circuits are Depicted With Dotted Lines)

BLOCK DIAGRAM

CONSTANT CURRENT SOURCE

SWITCHING SCHEMATIC

COMPLETE CIRCUIT SCHEMATIC

Differential CURRENT CONVERTER

MOTOROLA LINEAR/INTERFACE DEVICES

11-15
Regulator (Figure 15)
The regulator biases the entire MC1594 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the often adjust circuits. The regulated output voltage at pin 2 is approximately +4.3 V while the regulated voltage at pin 4 is approximately -4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that |V2| = |V4| = 1.0 mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 kΩ potentiometers and one 50 kΩ potentiometer connected between pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1594. Note that all constant sources are related to current I3 which is determined by R1. For best temperature performance, R1 should be 16 kΩ so that I3 = 0.5 mA for all applications.

Multiplier (Figure 15)
The multiplier section of the MC1594 (center section of Figure 15) is nearly identical to the MC1595 and is discussed in detail in Application Note AN-489, "Analysis and Basic Operation of the MC1595". The result of this analysis is that the differential output current of the multiplier is given by:

\[ I_O = \frac{2V_V \times V_Y}{R_X \times R_Y \times V_1} \]

Therefore, the output is proportional to the product of the two input voltages.

Differential Current Converter (Figure 15)
This portion of the circuitry converts the differential output current \( I_A \) of the multiplier to a single-ended output current \( I_0 \).

\[ I_0 = I_A \times 10 \]

The output current can be easily converted to an output voltage by placing a load resistor \( R_L \) from the output (pin 14) to ground (Figure 17) or by using an op-amp as a current-to-voltage converter (Figure 16). The result is in both circuits is that the output voltage is given by:

\[ V_O = \frac{2R_L \times V_X \times V_Y}{R_X \times R_Y \times V_1} \]

\[ I_0 = \frac{2V_X \times V_Y}{R_X \times R_Y \times V_1} \]

where \( K \) is the scale factor = \( \frac{2R_L}{R_X \times R_Y \times V_1} \)

DC Operation
Selection of External Components
For low frequency operation, the circuit of Figure 16 is recommended. For this circuit, \( R_Y = 20 \text{ kΩ}, R_X = 62 \text{ kΩ}, R_1 = 16 \text{ kΩ} \) and hence \( I_3 \approx 0.5 \text{ mA} \) Therefore, to set the scale factor, \( K \), equal to 1/10, the value of \( R_L \) can be calculated to be:

\[ K = 10 \times \frac{R_X R_Y V_1}{2} \]

\[ R_L = \frac{30 \text{ kΩ} \times 62 \text{ kΩ} \times 0.5 \text{ mA}}{2} \]

\[ R_L = 45.5 \text{ kΩ} \]

Thus, a reasonably accurate in scale factor can be achieved by making \( R_L \) a fixed 47 kΩ resistor. However, if it is desired...
that the scale factor be exact, \( R_L \) can be comprised of a fixed resistor and a potentiometer as shown in Figure 16. It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the \( V_X \) and \( V_Y \) input voltages are expected to be large, say \( 5 \) to \( 10 \) \( V \). Obviously with \( V_X = V_Y = 10 \) \( V \) and a scale factor of unity, the device could not hope to provide a 100 \( V \) output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set \( K = 1/2 \) or \( K = 1 \) or even \( K = 100 \). This can be accomplished by adjusting \( R_{X} \), \( R_{Y} \), and \( R_L \) appropriately.

The selection of \( R_L \) is arbitrary and can be chosen after resistors \( R_X \) and \( R_Y \) are found. Note in Figure 16 that \( R_L \) is 62 \( k\) \( \Omega \) while \( R_X \) is 30 \( k\) \( \Omega \). The reason for this is that the \( Y \)-side of the multiplier exhibits a second order non-linearity whereas the \( X \)-side exhibits a simple non-linearity. By making the \( R_Y \) resistor approximately twice the value of the \( R_X \) resistor, the linearity on both the \( X \) and \( Y \)-sides are made equal. The selection of the \( R_Y \) and \( R_Y \) resistor values is dependent upon the expected amplitude of the \( V_X \) and \( V_Y \) inputs. To maintain a specified linearity, resistors \( R_X \) and \( R_Y \) should be selected according to the following equations:

\[
R_Y > 3 \times V_X \text{ (max.) in } k\Omega \text{ when } V_Y \text{ is in volts}
\]

\[
R_Y > 6 \times V_Y \text{ (max.) in } k\Omega \text{ when } V_Y \text{ is in volts}
\]

For example, if the maximum input on the \( X \)-side is \( \pm 1 \) volt, resistor \( R_X \) can be selected to be 3 \( k\) \( \Omega \). If the maximum input on the \( Y \)-side is also \( \pm 1 \) volt, then resistor \( R_Y \) can be selected to be 6 \( k\) \( \Omega \) (6.2 \( k\) \( \Omega \) nominal value). If a scale factor of \( K = 10 \) is desired, the load resistor is found to be 47 \( k\) \( \Omega \). In this example, the multiplier provides a gain of 20 dB.

Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate currents-to-voltage converter. The output current of the multiplier flows through the feedback resistor \( R_L \) to provide a low impedance output voltage from the op-amp. Since the offset current and bias currents of the op-amp will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1556/MC1456 or MC1741/MC1741C are excellent choices for this application.

Since the MC1594 is capable of operation at much higher frequencies than the op-amp, the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the op-amp.

Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 \( \mu F \) in parallel with \( R_L \) should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op-amp might be employed using slightly heavier compensation than that recommended for unity-gain operation.

Offset Adjustment

The non-inverting input of the op-amp provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see offset and scale factor adjustment procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit in Figure 16 is:

A. Input Offset
   a. Connect oscillator (1 kHz), 5 Vpp sine wave to the "X" input (pin 8)
   b. Connect "Y" input (pin 10) to ground
   c. Adjust \( X \) offset potentiometer, P2, for an ac null at the output

B. Y Input Offset
   a. Connect oscillator (1 kHz), 5 Vpp sine wave to the "X" input (pin 8)
   b. Connect "Y" input (pin 9) to ground
   c. Adjust \( Y \) offset potentiometer, P1, for an ac null at the output

C. Output Offset
   a. Connect both "X" and "Y" inputs to ground
   b. Adjust output offset potentiometer, P3, until the output voltage \( V_o \) is zero volts dc

D. Scale Factor
   a. Apply 10 \( V \)dc to both the "X" and "Y" inputs
   b. Adjust P4 to achieve \(-10.00 \) \( V \) at the output
   c. Apply \(-10 \) \( Vdc \) to both "X" and "Y" inputs and check for \( V_o = -10.00 \) \( V \)

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1594 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinitely" resolution type rather than wirewound. Fine adjustments of balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

Temperature Stability

While the MC1594 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Proper design assures the direct dependence on \( R_X \), \( R_Y \), and \( R_L \) and indirect dependence on \( R \) through \( \beta \). Any circuit subjected to temperature variations should be evaluated with these effects in mind.

Bias Currents

The MC1594 multiplier, like most linear IC's, requires a dc bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs \( V_X \) and \( V_Y \) are able to supply the small bias current (\( \pm 0.5 \) \( \mu A \)) required. However, if the MC1594 is used in an ac mode of operation and capacitive coupling is used the value of resistor \( R \) may be any reasonable value up to 100 \( k\) \( \Omega \). For optimum noise and optimum temperature performance, the value of resistor \( R \) should be as low as practical.

Parasitic Oscillation

When large leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network
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is to reduce the "D" of the source tuned circuits which cause the oscillation.

Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

AC OPERATION

General

For ac operation, such as balanced modulation, frequency doubler, AGC, etc., the op-amp will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be ac-coupled and the dc voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17 shows a typical ac multiplier circuit with a scale factor $K = 1$. The resistor $R_X$ and $R_Y$ are chosen as outlined in the previous section, with $R_{LX}$ chosen to provide the required scale factor.

The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset voltage of the MC1594 is typically 17 $\mu$A and 35 $\mu$A maximum. Thus, the maximum output offset would be about 160 mV.

Bandwidth

The bandwidth of the MC1594 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance $C_0$ of 10 $\text{pF}$, the $3 \text{dB}$ bandwidth would be approximately 3.4 MHz. If the load resistors were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors $R_X$ and $R_Y$ and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of $R_X$ and $R_Y$ at high frequencies. Since the $R_Y$ resistor is approximately twice the value of the $R_X$ resistor, the zero associated with the "Y" input will occur approximately one octave below the zero associated with the "X" input. For $R_X > 30$ kΩ and $R_Y > 62$ kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 $\text{pF}$. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7 MHz, respectively.

It should be noted that the MC1594 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (s) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a dc voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an ac voltage on both the "X" and "Y" side, such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

In this brief discussion, it is evident that for ac applications, (1) the value of resistors $R_X$, $R_Y$, and $R_{LX}$ should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor $R_{LX}$ such that the dominant pole ($R_L$, $C_0$) cancels the input zero ($R_X$, 3.5 $\text{pF}$ or $R_Y$, 3.5 $\text{pF}$) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the ac signal. For ac applications requiring bandwidths greater than those specified for the MC1594, two other devices are recommended. For modulator-demodulator applications, the MC15956 may be used up to 100 MHz. For wideband multiplier applications, the MC15958 (using small collector loads and ac coupling) can be used.

Slew-Rate

The MC1594 multiplier is not slew-rate limited in the ordinary sense that an op-amp is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitations. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\Delta V_o = \frac{I_o}{s T}$$

Thus, if $C_L = 10 \text{ pF}$, the maximum slew rate would be:

$$\Delta V_o = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50 \text{ V/μs}$$

This can be improved if necessary by addition of an emitter-follower or other type of buffer.

Phase-Vector Error

All multipliers are subject to an error which is known as the phase-vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase-vector
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error is best explained by an example. If the "X" input is described in vector notation as
\[ X = A_x e^{j\theta_x} \]
and the "Y" input is described as
\[ Y = A_y e^{j\theta_y} \]
then the output product would be expected to be
\[ V_o = A_z e^{j\theta_z} \] (see Figure 18)

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by
\[ V_o = A_x A_y e^{j(\theta_x - \theta_y)} \]

Notice that the magnitude is correct but the phase angle of the product is in error. The vector, \( V_o \), associated with this error is the "phase-vector error". The starting fact about the phase-vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.05° will result in a 1% phase-vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase-vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase-vector error will represent a 1% amplitude error at the phase angle of interest.

**FIGURE 18 - PHASE VECTOR ERROR**

Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across \( R_x \) and \( R_y \) should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

DC APPLICATIONS

Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:
\[ V_o = K V^2 \]

where \( K \) is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:
\[ V_o = K V_x V_y(1 + K_x K_y) + V_o \] (See "Definitions" for an explanation of terms).

With \( V_x = V_o = V \) (squaring) and defining
\[ K_x = V_o + V_x = V_x \] or \( K_x + V_x = V_0 \)

The output voltage equation becomes
\[ V_o = K V^2 = K V_x K_y + V_x V_y + K_x K_y V_o \]

This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, \( K_x \) is determined by the internal offset. \( V_o \), but \( K_y \) is adjustable to the extent that the \( F_x + V_x \) term can be zeroed. Then the output offset adjustment is used to adjust the \( K_x K_y \) term and thus zero the remaining error terms. An ac procedure for nulling with three adjustments is:

A. AC Procedure:
1. Connect oscillator (1 kHz, 15 Vpp) to input
2. Monitor output at 2 kHz with tuned voltmeter and adjust F4 for desired gain (be sure to peak response of voltmeter)
3. Tune voltmeter to 1 kHz and adjust P1 for a minimum output voltage
4. Ground input and adjust P3 (offset adjustment) for zero volts d.c.
5. Repeat steps 1 through 4 as necessary.

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8. DC Procedure:
1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_O = 0.0$ Vdc.
2. Set $V_X = V_Y = 1.0$ V and adjust P1 (input offset potentiometer) such that the output voltage is -0.100 volts.
3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is -10.00 volts.
4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$ V.
Repeats steps 1 through 4 as necessary.

Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if $V_{X,Y}$ is allowed to go negative or, in some cases, if $V_{X,Y}$ approaches zero. Figure 20 illustrates why this is so. For $V_{X,Y} > 0$ the transfer function through the multiplier is non-inverting. Its output is fed to the inverting input of the op-amp. Thus, operation is in the negative feedback mode and the circuit is dc stable.

**FIGURE 20 - BASIC DIVIDE CIRCUIT USING MULTIPLIER**

Should $V_{X,Y}$ change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from $V_{X,Y}$ being near zero is a result of the transfer through the multiplier being near zero. The op-amp is then operating with a very high closed loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op-amp, exceeding the rated common mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op-amp to approximately ±10.7 V. Five percent tolerance, 10-Volt zeners are used to assure adequate output swing but still limit the output voltage of the op-amp to from exceeding the common mode input range of the MC1494.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set $V_{X,Y} = 0$ volts and adjust the output offset potentiometer (P3) until the output voltage ($V_O$) remains at some (not necessarily zero) constant value as $V_{X,Y}$ is varied between ±1.0 volt and ±10 volts.
2. Maintain $V_{X,Y}$ at 0 volts, set $V_O$ at ±10 volts and adjust the Y input offset potentiometer (P1) until $V_{X,Y}$ = 0 volts.
3. With $V_{X,Y} = V_O$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily ±10 volts) constant value as $V_{X,Y}$ = $V_O$ is varied between ±1.0 volt and ±10 volts.
4. Maintain $V_{X,Y} = V_O$ and adjust the scale factor potentiometer ($R_{S}$) until the average value of $V_{X,Y}$ is ±10 volts as $V_{X,Y}$ is varied between ±1.0 volt and ±10 volts.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denomi-
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**FIGURE 22 – BASIC SQUARE ROOT CIRCUIT**

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up.

This circuit too, may be adjusted in the closed-loop mode.

1. Set $V_V = -0.01$ Vdc and adjust P3 (output offset) for $V_V = 0.316$ Vdc.
2. Set $V_V = +0.9$ Vdc and adjust P2 ("X" adjust) for $V_V = +3$ Vdc.
3. Set $V_V = -0.1$ Vdc and adjust P4 (gain adjust) for $V_V = +10$ Vdc.

Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near zero volts input may prove very inaccurate, hence, it may be possible to adjust $V_V$ to 0 but only to within 100 to 400 mV of zero.

**AC APPLICATIONS**

Widband Amplifier With Linear AGC

If one input to the MC15944 is a dc voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the dc voltage. Hence, the multiplier can function as a dc coupled, wideband amplifier with linear AGC control.

In addition to the advantage of linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with zero volts dc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using carbon multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output-voltage swing capability and output impedance are unchanged with variations in AGC voltage.

The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier circuit (Volts) Exhibits a gain of approximately 70 dB. It is AGC through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter follower buffer has been added to extend the bandwidth in excess of 1 MHz.

**FIGURE 23 – SQUARE ROOT CIRCUIT**
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The output is suppressed-carrier double sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

\[ V_{o} = \frac{K}{2} (E_{1} \cos \omega_{1} t + E_{2} \cos \omega_{2} t) \]

where \( \omega_{m} \) is the modulation frequency and \( \omega_{c} \) is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

\[ V_{o} = \frac{E}{2} (\cos \omega_{m} t + \cos \omega_{c} t + \omega_{m} \cos \omega_{c} t) \]

Unlike many modulation schemes, which are non-linear in nature, the modulation which takes place when using the MC1594 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies: the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1594 configuration to perform this function.

**FIGURE 24 - WIDEBAND AMPLIFIER WITH LINEAR AGC**

Notice that the resistor values for \( R_{X} \), \( R_{Y} \), and \( R_{z} \) have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1594 and then lowering \( R_{X} \) and \( R_{Y} \) to achieve a gain of 1. The \( E_{m} \) can be as large as 1 volt peak and \( E_{m} \) as high as 2 volts peak. No output offset adjust is employed since we are interested only in the ac output components.

The input \( R_{S} \) are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 k\ohm output impedance and capacitive loading. Assuming a 6 pF load, the small-signal bandwidth is 6.5 MHz.

The circuit of Figure 25 will provide a typical carrier rejection of 70 dB from 10 kHz to 1.5 MHz.

**FIGURE 25 - BALANCED MODULATOR**

The adjustment procedure for this circuit is quite simple:

1. Place the carrier signal at pin 10. With no signal applied to pin 9, adjust potentiometer P1 such that an ac null is obtained at the output.
2. Place a modulation signal at pin 9. With no signal applied to pin 10, adjust potentiometer P2 such that an ac null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

**Frequency Doubler**

If for Figure 25 both inputs are identical:

\[ E_{m} = E_{c} = E \cos \omega t \]

Then the output is given by

\[ E_{o} = E_{m} R_{c} = E^{2} \cos^{2} \omega t \]

which reduces to

\[ E_{o} = \frac{E^{2}}{2} (1 + \cos 2\omega t) \]

This equation states that the output will consist of a dc term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires no filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2 MHz.

**Amplitude Modulator**

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the modu-
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D MODULATOR

\[
\begin{align*}
E_0 &= E \cdot \cos(2\pi ft) \\
\text{where } E &= \text{dc input offset adjust voltage} \\
\text{This expression} &\text{ can be written as} \\
E_0 &= E_0 \cdot \left(1 + M \cdot \cos(2\pi ft)\right) \\
M &= \frac{E_m}{E} \text{ modulation index} \\
\end{align*}
\]

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation, E_m. This is done by observing the output waveform and adjusting the input offset potentiometer, P1, until the output exhibits the familiar amplitude modulation waveform.

Phase Detector

If the circuit of Figure 26 has as its inputs two signals of identical frequency but having a relative phase shift, the output will be a dc signal which is directly proportional to the cosine of the phase difference as well as the double frequency term.

\[
\begin{align*}
e_0 &= E_0 \cdot \cos(2\pi ft) \\
e_m &= \frac{E_m}{2} \cdot \cos(2\pi ft) \\
e_0 &= E_0 \cdot \left(1 + M \cdot \cos(2\pi ft)\right) \\
or \quad e_{0m} &= \frac{E_m}{2} \cdot \cos(2\pi ft) \\
\end{align*}
\]

The addition of a simple low pass filter to the output which eliminates the second cosine term and return of R1 to an offset adjustment potentiometer will result in a dc output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

DEFINITIONS OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of this mystery, the following definitions and examples are presented.

Multiplier Transfer Function

The output of the multiplier may be expressed by this equation.

\[
V_o = K (V_x \cdot V_y) \cdot V_{off} \quad (V_{ref} = V_{off} \cdot V_{ref} + V_{dc})
\]

where \( K \) = scale factor (see 6.5)

\[
\begin{align*}
V_x &= \text{"x" input voltage} \\
V_y &= \text{"y" input voltage} \\
V_{off} &= \text{"x" input offset voltage} \\
V_{off} &= \text{"y" input offset voltage} \\
V_{dc} &= \text{"x" input offset adjust voltage} \\
\end{align*}
\]

\( V_{off} \) is the "y" input offset adjust voltage

\( V_{dc} \) is the output offset voltage

The voltage transfer characteristic below indicates "X", "Y" and output offset voltages.

\[
\text{FIGURE 26}
\]

Linarity

Linarity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full scale output and is measured for \( V_x \) and \( V_y \) separately or together using an "X-Y" plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.05% linearity means

\[
V_o = V_{dc} \times \frac{100}{1000} = 0.05 \text{ V}(100 \text{ VDC})
\]

Input Offset Voltage

The input offset voltage is defined from Equation (1). It is measured for \( V_x \) and \( V_y \) separately and is defined to be that dc input offset voltage ("X" or "Y") that will result in a maximum output when it is input into the other input ("Y" or "X") respectively. From Equation (1) we have

\[
V_{dc} = \frac{V_{dc}}{V_{ref}} \times V_{off} \\
\]

adjust \( V_{dc} \) so that it \( V_{dc} = V_{off} \cdot V_{dc} = 0 \)

Output Offset Current and Voltage

Output offset current (\( I_{dc} \)) is the dc current flowing in the output lead when \( V_x = V_{dc} = 0 \) and "X" and "Y" offset voltages are adjusted to zero.

Output offset voltage (\( V_{dc} \)) is

\[
V_{dc} = V_{dc} \times RL \\
\]

where \( RL \) is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting "X" and "Y" offset voltages to zero. Thus it includes input offset terms, an output offset term and a scale factor term.

Scale Factor

Scale factor is the \( K \) term in Equation (3). It determines the "gain" of the multiplier and is expressed approximately by the following equation:

\[
K = \frac{2RL}{R_x + R_y} \quad \text{where } R_x \text{ and } R_y \gg kT \\
\text{and } I \text{ is the current out of pin } 1
\]

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Total DC Accuracy
The total dc accuracy of a multiplier is defined as error in multiplier output with dc (±10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1594 because error terms can be nulled by the user.

Temperature Stability (Drift)
Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by re-adjusting the multiplier offsets and scale factors at each new temperature (see previous definitions and the adjustment procedure) and noting the change. Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by

\[ V_o = \pm |K_{O1} (TCK) (T - T) + |TCV_{o1} (T - T)| + |TCV_{off} (T - T)| \]

Total DC Accuracy Drift
This is the temperature drift in output voltage with 10 volts applied to each input. The output is adjusted to 10 volts at \( T_A = +25^\circ C \). Assuming initial offset voltages have been adjusted to zero at \( T_A = +25^\circ C \), then

\[ V_o = |K_{O1} (TCK) (T - T)| \pm |TCV_{o1} (T - T)| \pm |TCV_{off} (T - T)| \]

Power Supply Rejection
Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1 volt, 100 Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

Output Voltage Swing
Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load (input output offset is adjusted to zero).

If an op-amp is used, the multiplier output becomes a virtual ground - the swing is then determined by the scale factor and the op-amp selected.