

SHC298
SHC298A

Monolithic SAMPLE/HOLD AMPLIFIER

FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10 μ s ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20 μ Vrms
- RELIABLE MONOLITHIC CONSTRUCTION
- 10¹⁰ Ω INPUT RESISTANCE
- TTL/CMOS-COMPATIBLE LOGIC INPUT

DESCRIPTION

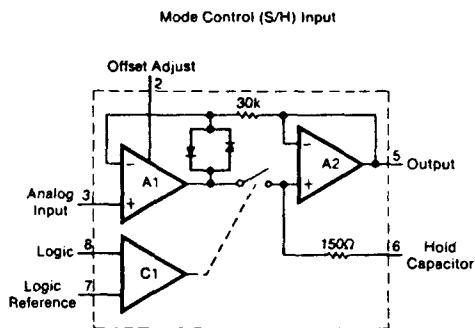
The SHC298 and SHC298A are high-performance monolithic sample/hold amplifiers featuring high DC accuracy with fast acquisition times and a low droop rate. Dynamic performance and holding performance can be optimized with proper selection of the external holding capacitor. With a 1000pF holding capacitor, 12-bit accuracy can be achieved with a 6 μ s acquisition time. Droop rates less than 5mV/min are possible with a 1 μ F holding capacitor.

These sample/holds will operate over a wide supply voltage ranging from \pm 5V to \pm 18V with very little change in performance. A separate Offset Adjust pin is used to adjust the offset in either the Sample or the Hold modes. The fully differential logic inputs have low input current, and are compatible with TTL, 5V CMOS, and CMOS logic families.

The SHC298AM is available in a hermetically sealed 8-pin TO-99 package and is specified over a temperature range from -25° C to $+85^{\circ}$ C. The SHC298JP and SHC298JU are 8-pin plastic DIP and SOIC packaged parts specified over 0° C to $+70^{\circ}$ C.

The SHC298AJP, specified over 0° C to $+70^{\circ}$ C, is available in an 8-pin plastic DIP. The SHC298A grade features improved Gain and Offset Error, improved drift over temperature, and faster Acquisition Time.

The SHC298 family is a price-performance bargain. It is well suited for use with several 12-bit A/D converters in data acquisition systems, data distribution systems, and analog delay circuits.



International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BURCORP • Telex: 66-6491

PDS-373C

SPECIFICATIONS

ELECTRICAL

Specifications at $T_j = +25^\circ\text{C}$, $\pm 15\text{V}$ supplies, 1000pF holding capacitor, $-11.5\text{V} \leq V_{in} \leq +11.5$, $R_L = 10\text{k}\Omega$, Logic Reference Voltage = 0V, and Logic Voltage = 2.5V unless otherwise noted.

PARAMETER	SHC298AM/JP/JU			SHC298AJP			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
ANALOG INPUT							
Resistance		10 ⁰			*		Ω
Bias Current ⁽¹⁾		10	50		*	25	nA
DIGITAL INPUT		Pin 7	Pin 8	Circuit State			
Mode Control Truth Table		0V 0V +2.4V +0.8V	+2.4V +0.8V +2.8V +2.8V	Sample (Track) Hold Hold Sample (Track)			
Mode Control and Mode Control Reference Input Current			10				μA
Differential Logic Threshold	0.8	1.4	2.4				V
TRANSFER CHARACTERISTICS							
ACCURACY (+25°C)							
Throughput Nonlinearity for Hold Time < 1ms		± 0.010	± 0.015		*	*	% of 20V
Gain		+1.0			*	*	V/V
Gain Error		± 0.004	± 0.010		± 0.001	± 0.005	%
Input Voltage Offset (adjust to zero) ⁽¹⁾		± 2	± 7		± 1	± 2	mV
Droop Rate ⁽¹⁾		± 30	± 200		*	± 100	$\mu\text{V/ms}$
Charge Offset ⁽²⁾		± 15	± 25		*	*	mV
Noise (rms) 10Hz to 100kHz		10	20		*	*	μV
Power Supply Rejection		± 25	± 100		*	*	$\mu\text{V/V}$
ACCURACY DRIFT							
Gain Drift		3	4		1	2	ppm/°C
Input Offset Drift		15	70		*	25	$\mu\text{V}/^\circ\text{C}$
Charge Offset Drift C = 1000pF		50	150		*	*	$\mu\text{V}/^\circ\text{C}$
Charge Offset Drift C = 10,000pF		20	50		*	*	$\mu\text{V}/^\circ\text{C}$
Droop Rate at $T_j = +85^\circ\text{C}$		1	10		*	*	mV/ms
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth, C = 1000pF	75	125		*	*		kHz
Full Power Bandwidth, C = 10,000pF	10	16		*	*		kHz
Output Slew Rate, C = 1000pF	7	10		*	*		V/ μs
Output Slew Rate, C = 10,000pF	1.4	2		*	*		V/ μs
Aperture Time: Negative Input Step		200	250		*	*	ns
Positive Input Step		150	200		*	*	ns
Acquisition Time (C = 1000pF): to $\pm 0.01\%$, 10V step		6	10		*	*	μs
to $\pm 0.01\%$, 20V step		8	12		*	*	μs
to $\pm 0.1\%$, 10V step		5	9		4	6	μs
to $\pm 0.1\%$, 20V step		7	11		*	*	μs
Sample/Hold Transient: Peak Amplitude		180			*	*	mV
Settling to 1mV		1.0	1.5		*	*	μs
Feedthrough (Response to 10V Input Step)		± 0.007	± 0.015		± 0.004	± 0.0075	% of 20V
OUTPUT							
ANALOG OUTPUT							
Voltage Range	± 11.5				*		V
Current Range	± 2				*		mA
Impedance (in hold mode)		0.5	4		*	*	Ω
POWER SUPPLY							
Rate Voltage		± 15			*	*	VDC
Range	± 5.0		± 18		*	*	VDC
Current ⁽¹⁾		± 4.5	± 6.5		*	*	mA

* Same as specifications for SHC298AM/JP/JU

NOTES: (1) These parameters guaranteed over a supply voltage range of $\pm 5\text{V}$ to $\pm 18\text{V}$. (2) Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01 μF hold capacitor. Magnitude of the charge offset is inversely proportional to hold capacitor value.

V_{CC} = 0V, and Logic Voltage =

UNIT	MAX	UNITS
25		Ω nA
Output State		
Idle (Track)		
Hold		
Hold		
Idle (Track)		
		μA V

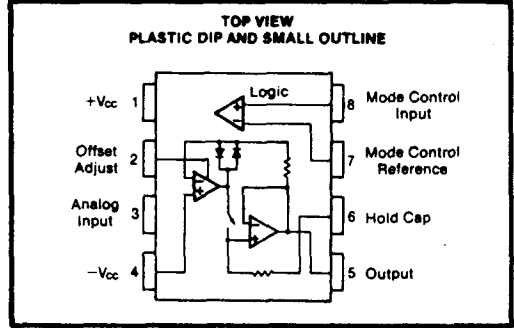
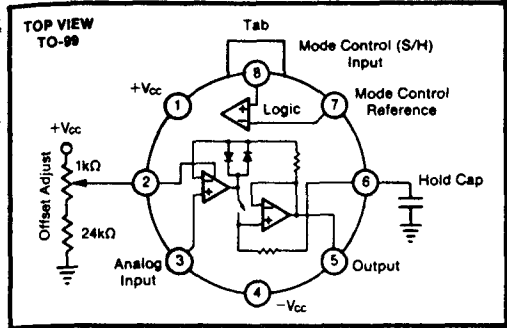
•	% of 20V
±0.005	V/V
±2	%
±100	mV
•	μV/ms
•	mV
•	μV
•	μV/V
•	ppm/°C
•	μV/°C
•	μV/°C
•	μV/°C
•	mV/ms

•	kHz
•	kHz
•	V/μs
•	V/μs
•	ns
•	ns
•	μs
•	μs
•	μs
•	mV
•	μs
±0.0075	% of 20V

•	V
•	mA
•	Ω
•	VDC
•	VDC
•	mA

to stray capacitive coupling and a 0.01μF hold capacitor.

PIN DESIGNATIONS



MECHANICAL

"P" Package—Plastic DIP

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

Numbers may not be marked on package. Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.355	.400	9.03	10.16
A ₁	.340	.384	8.64	9.78
B	.230	.290	5.85	7.37
B ₁	.200	.250	5.08	6.36
C	.120	.200	3.05	5.08
D	.015	.023	0.38	0.58
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	18°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

θ_M = 130° C/W

"U" Package—Small Outline Surface Mount

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.201	4.70	5.11
A ₁	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B ₁	.130	.149	3.30	3.78
C	.054	.145	1.37	3.69
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

θ_M = 150° C/W

"M" Package—TO-99

NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane. Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.185	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.180	2.79	4.08
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

θ_M = 150° C/W
θ_{JC} = 45° C/W

SHC298/298A

SAMPLE/HOLD AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V	Output Short Circuit Duration	Indefinite
Power Dissipation (Package Limitation)	500mW	Hold Capacitor Short Circuit Duration	10s
Junction Temperature, $T_{j, max}$		Lead Temperature (soldering, 10s)	300°C
AM	125°C	NOTE: (1) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.	
JP, JU	100°C		
Operating Temperature Range	-25°C to +85°C		
Storage Temperature Range	-65°C to +150°C		
Input Voltage	Equal to Supply Voltage		
Logic-to-Logic Reference Differential Voltage ⁽¹⁾	+7V, -30V		

BURN-IN SCREENING

Burn-in screening is available for both plastic and TO-99 metal can packages. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C

TO-99 "-BI" models: +125°C

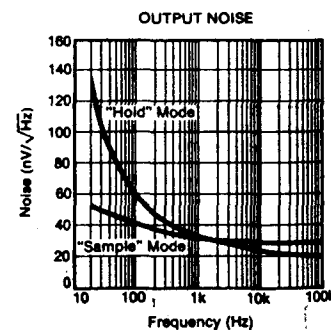
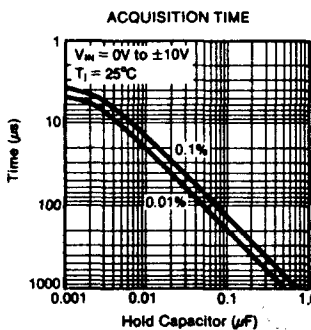
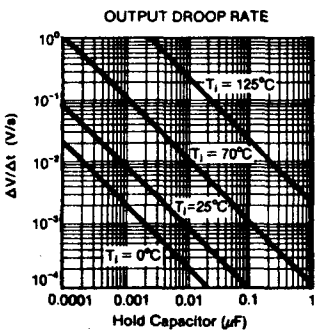
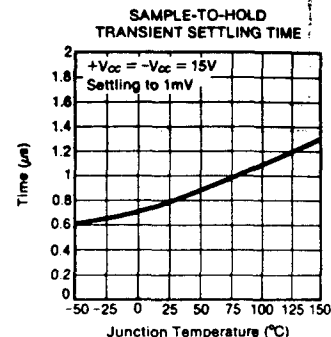
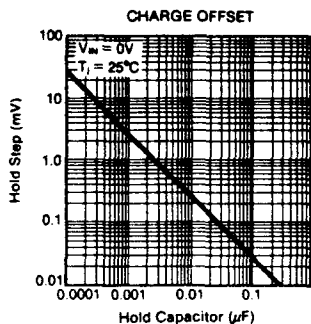
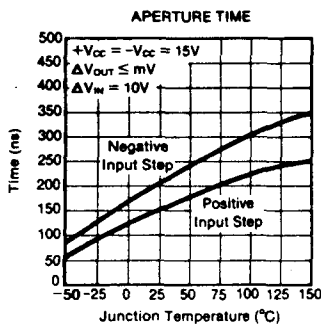
All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ORDERING INFORMATION

Model	Package	Temperature Range
SHC298AM	TO-99	-25°C to +85°C
SHC298JP	8-pin DIP	0°C to +70°C
SHC298JU	8-lead SOIC	0°C to +70°C
SHC298AJP	8-pin DIP	0°C to +70°C

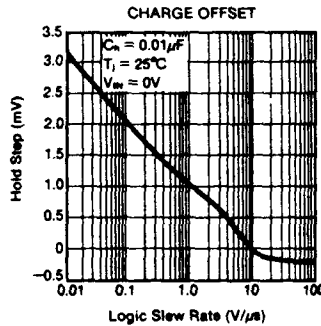
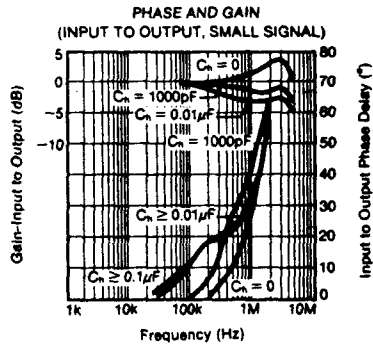
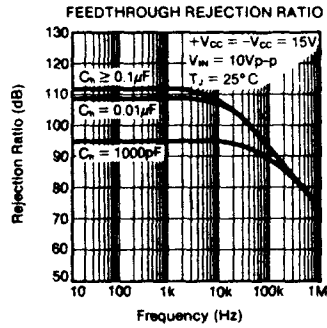
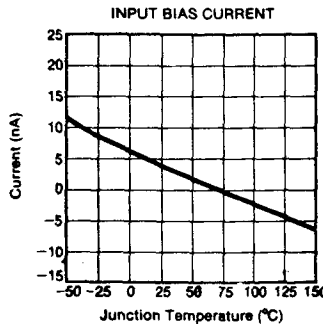
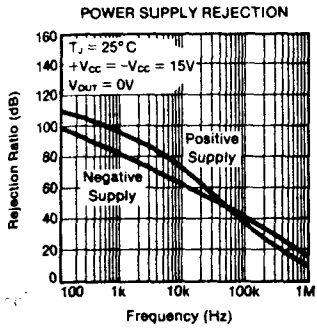
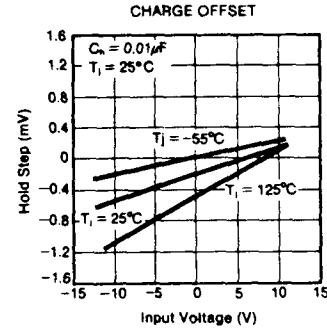
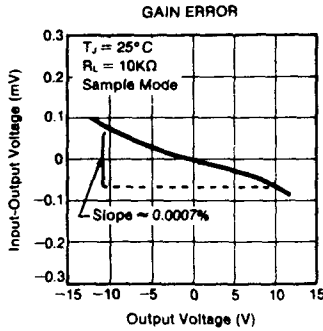
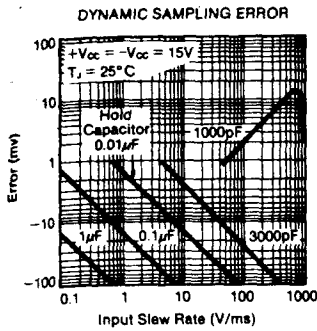
BURN-IN SCREENING OPTION		
See text for details.		
Model	Package	Temperature Range
SHC298AM-BI	TO-99	-25°C to +85°C
SHC298JP-BI	8-pin DIP	0°C to +70°C
SHC298JU-BI	8-lead SOIC	0°C to +70°C
SHC298AJP-BI	8-pin DIP	0°C to +70°C

TYPICAL PERFORMANCE CURVES



Indefinite
10s
300°C

exceed the
pins may be
the circuit.
pins must
V above the



DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Throughput nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, 1ms of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000pF holding capacitor, 10V input changes, 10 μs acquisition time, and 1ms Hold time (see Figure 1).

GAIN ACCURACY

Gain Accuracy is the difference between Input and Output voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

Feedthrough is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

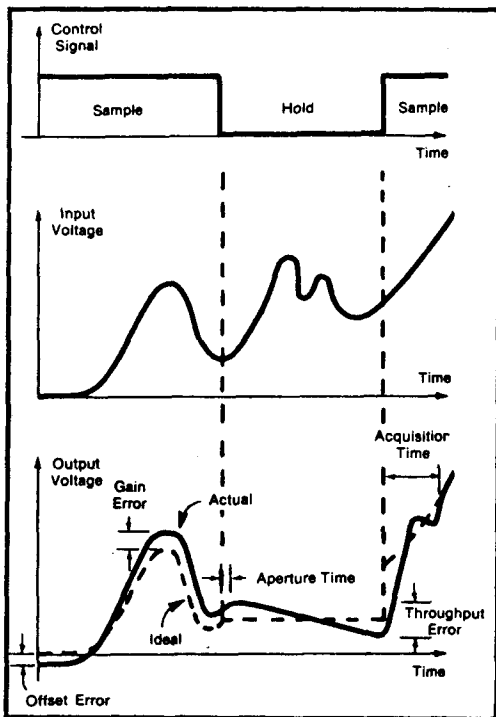


FIGURE 1. Sample Hold Errors.

APERTURE TIME

Aperture Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME

Acquisition Time is the time required for the sample/hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

CHARGE OFFSET

Charge Offset is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as teflon, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce charge offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample/hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001 μF capacitor. With a capacitor of 0.01 μF the droop will reduce to approximately 2.5 $\mu\text{V}/\text{ms}$ and the charge offset to approximately 1.5 mV. The behavior of acquisition time with changes in external capacitance is shown in the Typical Performance Curves.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001 μF capacitor is used, it will not be possible to adjust the full offset error at the sample/hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298 may be used to hold data for conversion with an analog-to-digital converter or used to provide Pulse Amplitude Modulation (PAM) data output (see Figures 2 and 3).

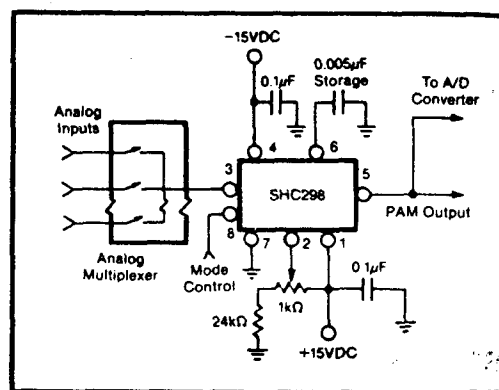


FIGURE 2. Data Acquisition.

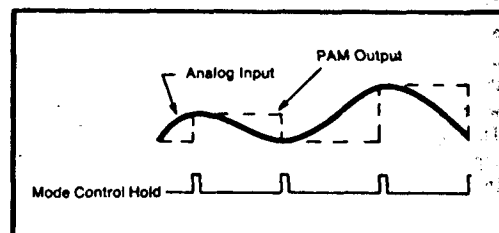


FIGURE 3. PAM Output.

DATA DI
The SHC
to-analog
(see Figur

Digital
Inputs

Di
In

FIGURE

TEST SY

The SHC
acquire ar
for other
digital vol

With a 0.1
10 second
capacitor,
with less t

CAPACIT

298 i
may
should be