

Supplementary information on firmware and hardware for “Photon counting, sensor corrections, and lifetime imaging for improved detection in two-photon microscopy”

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Fast Discriminator Circuitry

We created a discriminator circuitry that allows for counting at speeds of 350 MHz and can be integrated into a single board which also contains the complex programmable logic device (CPLD) and auxiliary circuitry (**Fig. S1**). As an alternative strategy, fast discrimination can be accomplished with a commercial discriminator device (PRL-350TTL, Pulse Research Lab), albeit with the lower maximum effective counting rate of 280 MHz.

CPLD Circuitry

Critical to the implementation of our counting device is the use of an ultrafast CPLD, which allows digital counting and timing circuitry to be created in software and then downloaded into the device’s firmware. We use the Lattice IspMach LC4256V chip, which allows for 256 logic devices and runs at a maximum effective speed of greater than 400 MHz. The CPLD circuitry is created using ispLEVER Classic, and flashed to the chip using a standard parallel port interface.

Use of a CPLD results in a minimal digital hardware, since the counters, time gating, and delay line for synchronization with the laser pulses can all be implemented in the firmware of a single chip.

Fast counters. There are many possible ways to implement digital counters. In the case of our photon counters, we designed for the following requirements. (i) The counters should be able to operate as quickly as possible, to allow for the possibility of multiple pulses within one laser repetition. (ii) The counters should not miscount in the case of two closely spaced pulses. (iii) The counters should avoid misreads by the computer (PC), since a pulse can occur even during a read, which could result in an erroneous value if the counter has not settled.

The solution is to use a dual ripple counter scheme (**Fig. S2**). Ripple counters are fast and stable, but have the disadvantage of a slower settling time, since only one flip-flop can change state at a time, and changes of more significant bits “ripple” through the system. Time multiplexing two separate counters allows for the fastest possible counting speed, without the

possibility of counting or read errors. The dead time of this system is negligible, on the order of 1 ns.

Programmable digital delay line and multi-bin time gating. In addition to functioning as a high-speed counter, the CPLD can be programmed to sort the incoming photon pulses into separate counters according to the arrival time relative to a synchronization signal (**Fig. S3A**) and thus execute fluorescent lifetime imaging microscopy (FLIM). The synchronization signal is derived from the laser pulse, and is sent through a series of gates that implement a create a user-selectable delay lines. The delay line is set so that photon counts immediately following the excitation pulse fall into the first bin. In this configuration, a total of six time gated four-bit counters are used (**Fig. S3B,C**). The computer acquires this data as values from three eight-bit counters, and sorts and analyses the data in post-processing.

The overall design is similar to the standard photon counting setup, except that the FLIM design can be run in one of three modes, which are selectable using a thumbwheel on the counting device (**Fig. S3B**). Setting the thumbwheel to 0 implements the standard photon counting mode, using a single 8-bit counter. This is useful to obtain an overall image of the sample, or in cases where FLIM is not necessary or desired. Setting the thumbwheel to 1 implements a single 4-bit counter on channel one. In this mode, only counts from the first time bin (the bin which catches the initial excited photons) are displayed. This is useful for adjusting the delay lines on the laser_sync signal, and insuring that the counters do not rollover and exceed the maximum of 15 counts possible for a 4-bit counter. And finally, setting the thumbwheel to 2 implements the full FLIM mode. In this mode, the six time gated channels, with 4-bits each, are multiplexed into the three imaging channels of the scope.

Counting the number of pulses per laser repetition. The CPLD can be reconfigured to give the distribution of counts per laser repetition, in addition to acquiring the full number of counts. The key additional component is the use of flip-flops, configured so that the counters will inactivate after receiving either one or two pulses (**Fig. S4**). The flips-flops are reset by the laser sync signal. Because pulses arriving exactly during the reset can be missed, the laser-sync delay is adjusted to give the maximum number of pulses in the gated bins, thus ensuring the reset happens immediately before a new laser repetition, after the fluorescence has died out.

The number of times zero pulses occurred, r_0 , is calculated by subtracting the number of time one or more pulse occurred from the number of laser repetitions per pixel. Similarly, the number of times exactly one pulse occurred, r_1 , is calculated by subtracting the number of times two or more pulses occurred from the number of times one or more pulses occurred.

Supplemental Figure Captions

Figure S1. Fast discriminator The discriminator threshold is set over the range of ± 2.5 V by a front panel 10-turn potentiometer. The threshold voltage can be monitored at a front panel BNC. The discrimination is accomplished by an ultrafast comparator integrated circuit, (MAX9600, Maxim IC), which takes the input signal and the discrimination threshold voltage as inputs. The differential ECL output from the discriminator is converted to a ground referenced signal through a transformer and then amplified (GVA-84+, Mini-Circuits). The trimmer and inductor network provide power to the amplifier, and level-shift the output for TTL compatibility. Two amplifiers (HFA-1112IBZ, Intersil) provide buffered outputs for monitoring the input and output signals respectively.

Figure S2. Counting circuitry for lifetime imaging. Shown is an 8-bit counter for one channel. At any given time, only one of the counters is active, and the contents of the other inactive counter are connected to the output pins through a multiplexer. A rising edge of the SCANCLK from the data acquisition card means that a read has been completed; this clears the inactive counter, then switches the active and inactive counters after a short delay, giving time for the previously active counter to settle before being the next read cycle. The result is a counter which can operate up to 400 MHz, while avoiding the miscounting and read errors. For a typical photon counting setup, this is all the CPLD circuitry that is needed. In practice, three output channels can easily fit onto one CPLD chip. Four-bit counters (not shown) are identical, with the exception of four rather than eight flip-flops, and a 4-bit rather than 8-bit multiplexer at the output.

Figure S3. Time delay and gating circuitry. (A) To capture lifetime decay information, a series of six gates are opened in sequence after a laser sync signal indicates the initial fluorescent excitation. In order to time the gates so that the initial fluorescence signal (after excitation) falls in the first gate, a digital delay line made from buffer gates is used. The length of the delay line is controlled by a 4-bit switch connected to the device (DLA), which allows the delay line to be tapped after a user-selected number of gates. The delayed laser_sync signal then uses a series of flip-flops to open six gates in sequence. The time between the opening of successive gates, as well as the active time of a given gate, is 1.5 ns. **(B)** When using the counting hardware for lifetime imaging, the counters can be run in one of three modes, selectable by a thumbwheel

switch connected to the device. With the wheel set to 0, the photomultiplier tube (PMT) signal is connected to an 8 bit counter, in the standard configuration. With the wheel set to 1, channel 1 displays the result from the first time bin only. This is useful for setting the delay between the laser_sync signal and the PMT. With the wheel set to 1, the first 4 bits of channel 1 are used for time gated counter 1, and the remaining 4-bits are used for time gated counter 2. (C) In addition, four additional 4-bit counters are used to count pulses from the time bins 3, 4, 5, and 6.

Figure S4. Measuring counts per laser repetition. In this configuration, three 8-bit counters are used. The upper counter records the number of times that one or more count occurred during a laser repetition. The middle counter, records the number of times two or more counts occurred during a laser repetition, and the third counter counts the full number of pulses. The PMT input to the upper two counters employ flip-flops, which are reset by the laser sync signal, to limit the number of counts per laser repetition.