DAQ

PCI-6110/6111 User Manual

Multifunction I/O Devices for PCI Bus Computers

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About This Manual

This manual describes the electrical and mechanical aspects of the 611*X* family of devices and contains information concerning their operation and programming.

The 611*X* family of devices includes:

- PCI-6110
- PCI-6111

Your 611*X* device is a high-performance multifunction analog, digital, and timing I/O device for PCI bus computers. Supported functions include analog input, analog output, digital I/O, and timing I/O.

Conventions

The following conventions appear in this manual:

<>	Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DBIO<3..0>.
	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.
611*X*	This refers to either the PCI-6110 or PCI-6111 device.
bold	Bold text denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.
Macintosh	Macintosh refers to all Macintosh OS computers with PCI bus, unless otherwise noted.

`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.
NI-DAQ	NI-DAQ refers to the NI-DAQ driver software for Macintosh or PC compatible computers unless otherwise noted.
PC	Refers to all PC AT series computers with PCI bus unless otherwise noted.
SCXI	SCXI stands for Signal Conditioning eXentsions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National instruments plug-in DAQ devices.

National Instruments Documentation

The *PCI-6110/6111 User Manual* is one piece of the documentation set for your DAQ system. You could have any of several types of documentation depending on the hardware and software in your system. Use the documentation you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware documentation—This documentation has detailed information about the DAQ hardware that plugs into or is connected to your computer. Use this documentation for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software documentation—You may have both application software and NI-DAQ software documentation. National Instruments application software includes ComponentWorks, LabVIEW, LabWindows/CVI, Measure, and VirtualBench. After you set up your hardware system, use either your application software documentation or the NI-DAQ documentation to help you write your application. If you have a large, complicated system, it is worthwhile to look through the software documentation before you configure your hardware.

- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- SCXI chassis manuals—If you are using SCXI, read these manuals for maintenance information on the chassis and installation instructions.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *DAQ-STC Technical Reference Manual*
- National Instruments Application Note 025, *Field Wiring and Noise Considerations for Analog Signals*
- *PCI Local Bus Specification Revision 2.0*

1 Introduction

This chapter describes your 611*X* device, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack your 611*X* device.

About the 611*X* Devices

Thank you for buying a National Instruments PCI-6110/6111 device. Your 611*X* device is a completely Plug and Play, multifunction analog, digital, and timing I/O device for PCI bus computers. The 611*X* device features a 12-bit ADC per channel with four or two simultaneously sampling analog inputs, 16-bit DACs with voltage outputs, eight lines of TTL-compatible digital I/O, and two 24-bit counter/timers for timing I/O. Because the 611*X* device has no DIP switches, jumpers, or potentiometers, it is easily software-configured and calibrated.

The 611*X* device is a completely switchless and jumperless data acquisition (DAQ) device for the PCI bus. This feature is made possible by the National Instruments MITE bus interface chip that connects the device to the PCI I/O bus. The MITE implements the PCI Local Bus Specification so that the interrupts and base memory addresses are all software configured.

The 611*X* device uses the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate.

Often with DAQ devices, you cannot easily synchronize several measurement functions to a common trigger or timing event.
The 611*X* device has the Real-Time System Integration (RTSI) bus to solve this problem. The RTSI bus consists of our RTSI bus interface and a ribbon

cable to route timing and trigger signals between several functions on as many as five DAQ devices in your computer.

Detailed specifications of the 611*X* device are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use the 611*X* device, you will need the following:

- ❑ Either the PCI-6110 or PCI-6111 device
- ❑ *PCI-6110/6111 User Manual*
- ❑ One of the following software packages and documentation:
  - ComponentWorks
  - LabVIEW for Macintosh
  - LabVIEW for Windows
  - LabWindows/CVI for Windows
  - Measure
  - NI-DAQ for PC Compatibles
  - VirtualBench
- ❑ Your computer

Software Programming Choices

You have several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use National Instruments application software, NI-DAQ, or register-level programming.

National Instruments Application Software

ComponentWorks contains tools for data acquisition and instrument control built on NI-DAQ driver software. ComponentWorks provides a higher-level programming interface for building virtual instruments through standard OLE controls and DLLs. With ComponentWorks, you can use all of the configuration tools, resource management utilities, and interactive control utilities included with NI-DAQ.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to NI-DAQ software.

LabWindows/CVI features interactive graphics, state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

VirtualBench features virtual instruments that combine DAQ products, software, and your computer to create a stand-alone instrument with the added benefit of the processing, display, and storage capabilities of your computer. VirtualBench instruments load and save waveform data to disk in the same forms that can be used in popular spreadsheet programs and word processors.

Using ComponentWorks, LabVIEW, LabWindows/CVI, or VirtualBench software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages or National Instruments application software, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

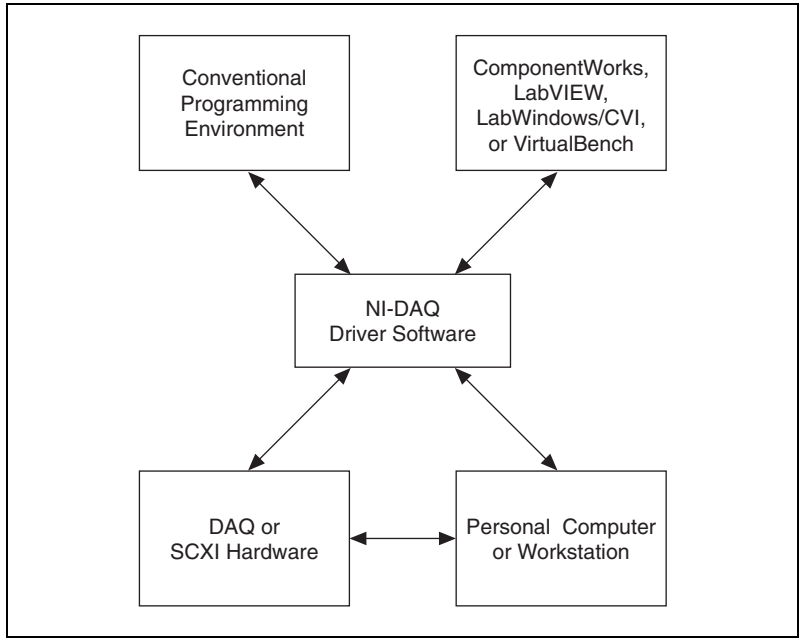


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient, and is not recommended for most users.

Even if you are an experienced register-level programmer, using NI-DAQ or application software to program your National Instruments DAQ hardware is easier than, and as flexible as, register-level programming, and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with the 611*X* device, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies
- Connector blocks, shielded and unshielded 50- and 68-pin screw terminals
- RTSI bus cables
- Low channel-count signal conditioning modules, devices, and accessories, including conditioning for strain gauges, RTDs, and relays

For more specific information about these products, refer to your National Instruments catalogue or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change device interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

Mating connectors and a backshell kit for making custom 68-pin cables are available from National Instruments.

The following list gives recommended part numbers for connectors that mate to the I/O connector on the 611*X* device:

- Honda 68-position, solder cup, female connector (part number PCS-E68FS)
- Honda backshell (part number PCS-E68LKPA)

Unpacking

The 611*X* device is shipped in an antistatic package to prevent electrostatic damage to the device. Electrostatic discharge can damage several components on the device. To avoid such damage in handling the device, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the device from the package.
- Remove the device from the package and inspect the device for loose components or any other sign of damage. Notify National Instruments if the device appears damaged in any way. Do *not* install a damaged device into your computer.
- *Never* touch the exposed pins of connectors.

2

Installation and Configuration

This chapter explains how to install and configure your 611*X* device.

Software Installation

Install your software before you install the 611*X* device. Refer to the appropriate release notes indicated below for specific instructions on the software installation sequence.

If you are using LabVIEW, LabWindows/CVI, or other National Instruments application software packages, refer to the appropriate release notes. After you have installed your application software, refer to your NI-DAQ release notes and follow the instructions given there for your operating system and application software package.

If you are using NI-DAQ, refer to your NI-DAQ release notes. Find the installation section for your operating system and follow the instructions given there.

Hardware Installation

You can install the 611*X* device in any available expansion slot in your computer. However, to achieve best noise performance, leave as much room as possible between the 611*X* device and other devices and hardware. The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings.

1. Turn off and unplug your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the 611*X* device into a 5 V PCI slot. Gently rock the device to ease it into place. It may be a tight fit, but *do not force* the device into place.
5. If required, screw the mounting bracket of the 611*X* device to the back panel rail of the computer.

6. Replace the cover.
7. Plug in and turn on your computer.

The 611*X* device is installed. You are now ready to configure your software. Refer to your software documentation for configuration instructions.

Device Configuration

Due to the National Instruments standard architecture for data acquisition and the PCI bus specification, the 611*X* device is completely software configurable. You must perform two types of configuration on the 611*X* device—bus-related and data acquisition-related configuration.

The 611*X* device is fully compatible with the industry standard *PCI Local Bus Specification Revision 2.0*. This allows the PCI system to automatically perform all bus-related configurations and requires no user interaction. Bus-related configuration includes setting the device base memory address and interrupt channel.

Data acquisition-related configuration includes such settings as analog input coupling and range, and others. You can modify these settings using NI-DAQ or application level software, such as ComponentWorks, LabVIEW, LabWindows/CVI, and VirtualBench.

3

Hardware Overview

This chapter presents an overview of the hardware functions on your 611*X* device. Figure 3-1 shows a block diagram for the PCI-6110 device.

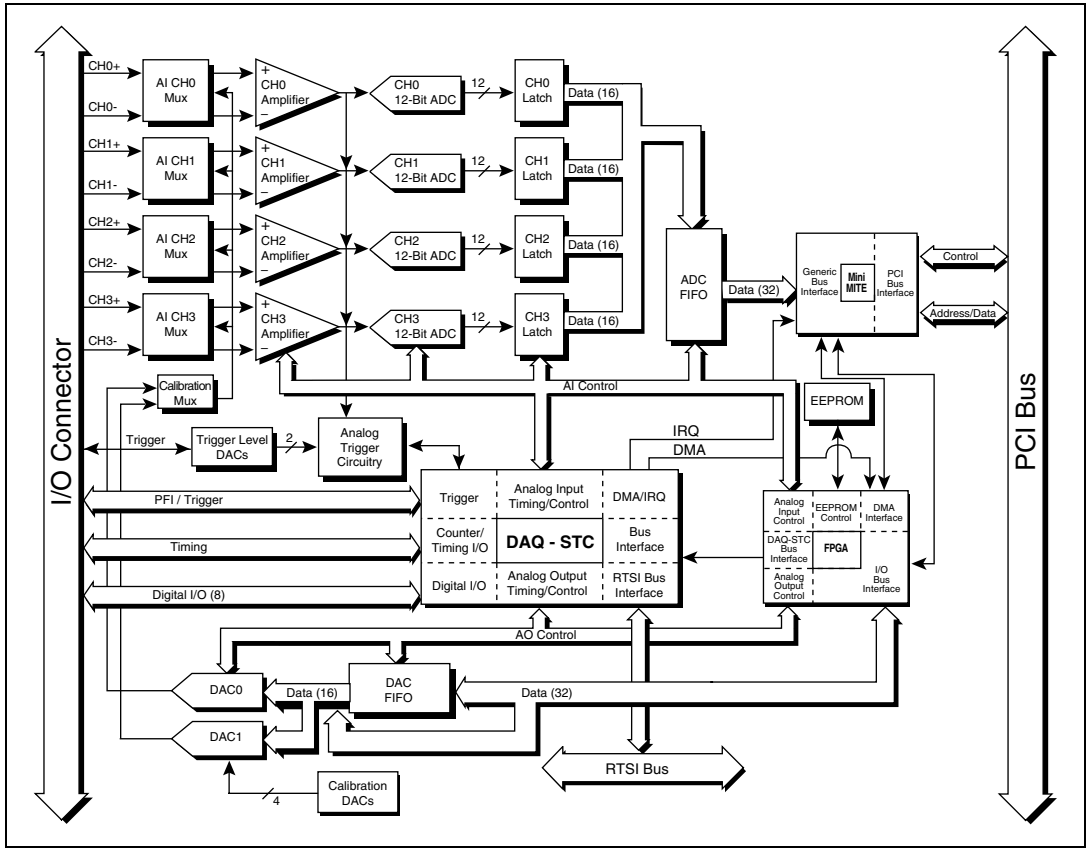


Figure 3-1. PCI-6110 Block Diagram

Figure 3-2 shows a block diagram for the PCI-6111 device.

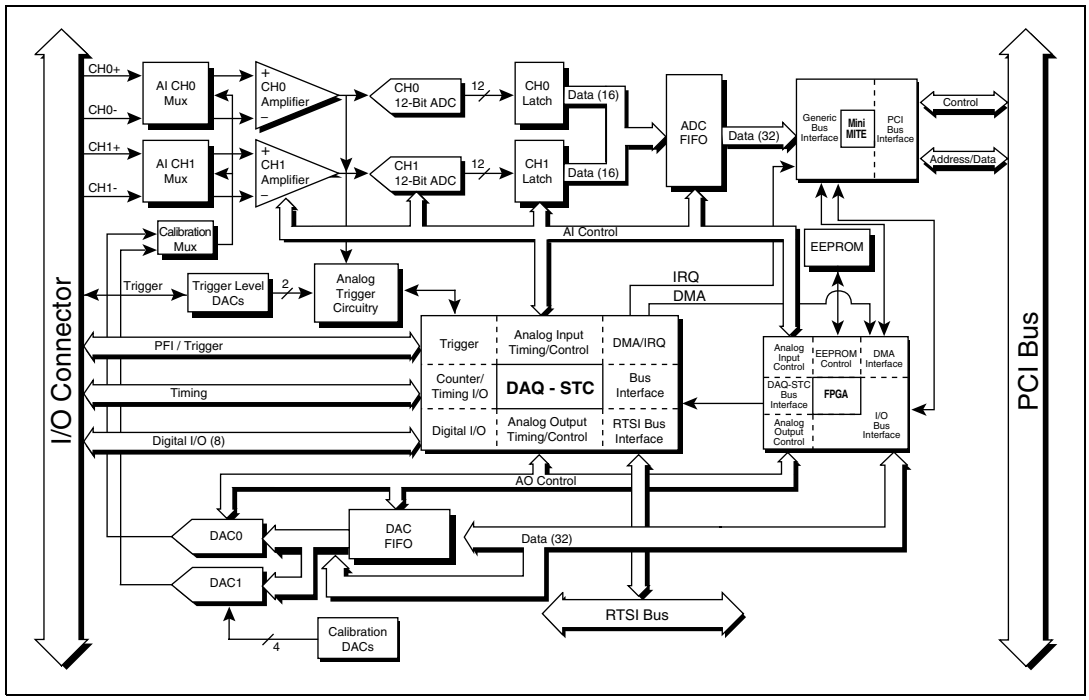


Figure 3-2. PCI-6111 Block Diagram

Analog Input

The analog input section for the 611*X* device is software configurable. You can select different analog input configurations through application software. The following sections describe in detail each of the analog input categories.

Input Mode

The 611*X* device supports only differential inputs (DIFF). The DIFF input configuration provides up to four channels on the PCI-6110 device and up to two channels on the PCI-6111 device.

A channel configured in DIFF mode uses two analog channel input lines. One line connects to the positive input of the device programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA. For more information about DIFF input configuration,

refer to the *Analog Input Signal Connections* section in Chapter 4, *Signal Connections*, which contains diagrams showing the signal paths for DIFF input.

Input Polarity and Input Range

The 611*X* device has bipolar inputs only. Bipolar input means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. These devices have a bipolar input range of 20 V (±10 V).

You can program range settings on a per channel basis so that you can configure each input channel uniquely.

The software-programmable gain on these devices increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. They have gains of 0.2, 0.5, 1, 2, 5, 10, 20, and 50, and are suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-1 shows the overall input range and precision according to the gain used.

Table 3-1. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range[1]	Precision[2]
–10 to +10 V	0.2	–50 to +50 V	24.41 mV
	0.5	–20 to +20 V	9.77 mV
	1.0	–10 to +10 V	4.88 mV
	2.0	–5 to +5 V	2.44 mV
	5.0	–2 to +2 V	976.56 µV
	10.0	–1 to +1V	488.28 µV
	20.0	–500 to +500 mV	244.14 µV
	50.0	–200 to +200 mV	97.66 µV

[1] **Warning:** The 611*X* is not designed for input voltages greater than 42 V, even if a user-installed voltage divider reduces the voltage to within the input range of the DAQ device. Input voltages greater than 42 V can damage the 611*X*, any device connected to it, and the host computer. Overvoltage can also cause an electric shock hazard for the operator. National Instruments is NOT liable for damage or injury resulting from such misuse.

[2] The value of 1 LSB of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

Note: See Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

The range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, match the input range as closely as possible to the expected range of the input signal.

Input Coupling

You can configure the 611*X* device for either AC or DC input coupling on a per channel basis. Use AC coupling when your AC signal contains a large DC component. If you enable AC coupling, you remove the large DC offset for the input amplifier and amplify only the AC component. This makes effective use of the ADC dynamic range.

Dither

Dither adds approximately 0.5 LSBrms of white Gaussian noise to the signal to be converted by the ADC. This addition is useful for applications involving averaging to increase the resolution of the 611*X* device, as in calibration or spectral analysis. In such applications, noise modulation is decreased and differential linearity is improved by the addition of the dither. When taking DC measurements, such as when checking the device calibration, you should average about 1,000 points to take a single reading. This process removes the effects of quantization and reduces measurement noise, resulting in improved resolution.

Figure 3-3 illustrates the effect of dither on signal acquisition. Figure 3-3a shows a small (±4 LSB) sine wave acquired without dither. The ADC quantization is clearly visible. Figure 3-3b shows what happens when 50 such acquisitions are averaged together; quantization is still plainly visible. In Figure 3-3c, the sine wave is acquired with dither. There is a considerable amount of visible noise. But averaging about 50 such acquisitions, as shown in Figure 3-3d, eliminates both the added noise and the effects of quantization. Dither has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.

You cannot disable dither on the 611*X* device. This is because the ADC resolution is so fine that the ADC and the PGIA inherently produce almost 0.5 LSBrms of noise. This is equivalent to having a dither circuit that is always enabled.

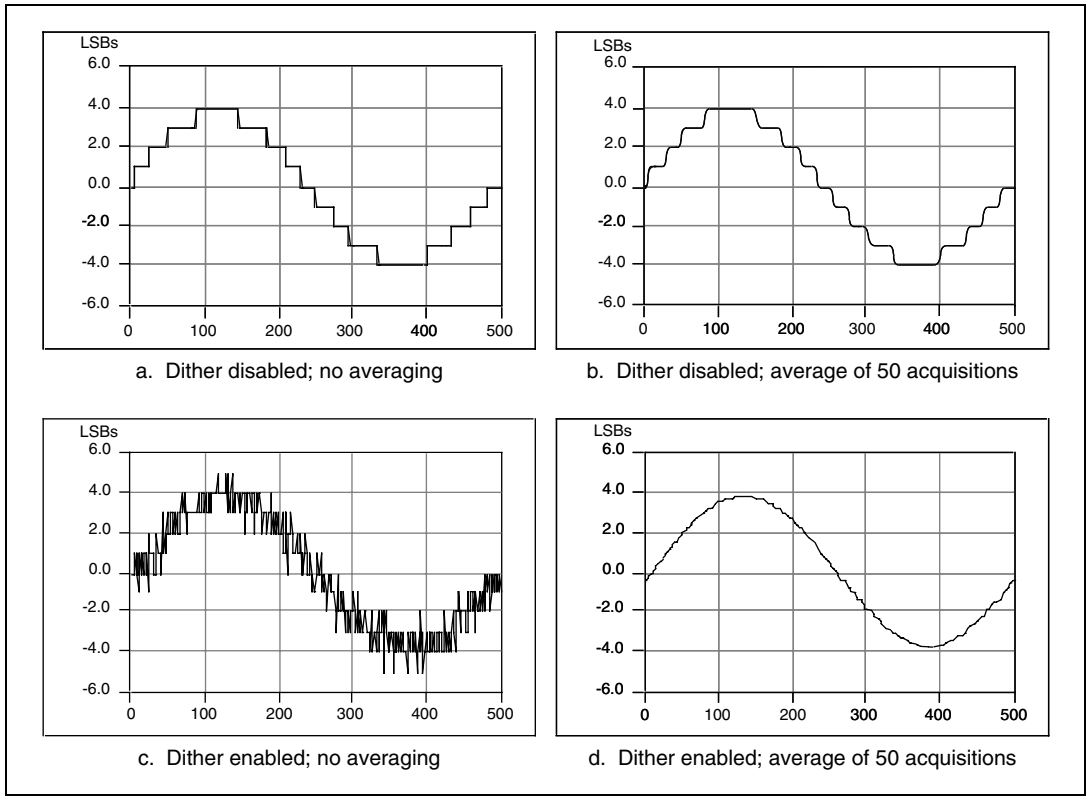


Figure 3-3. Effects of Dither on Signal Acquisition

Analog Output

The 611*X* device supplies two channels of analog output voltage at the I/O connector. The range is fixed at bipolar ±10 V.

Analog Trigger

In addition to supporting internal software triggering and external digital triggering to initiate a data acquisition sequence, these devices also support analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA on any of the channels, as shown in Figures 3-4 and 3-5. The trigger-level range for the direct analog channel is ±10 V in 78 mV steps for the 611*X* device. The range for the post-PGIA trigger selection is simply the full-scale range of the selected channel, and the resolution is that range divided by 256.

Note The PFI0/TRIG1 pin is an analog input when configured as an analog trigger. Therefore, it is susceptible to crosstalk from adjacent pins, which can result in false triggering when the pin is left unconnected. To avoid false triggering, make sure this pin is connected to a low-impedance signal source (less than 1 kΩ source impedance) if you plan to enable this input via software.

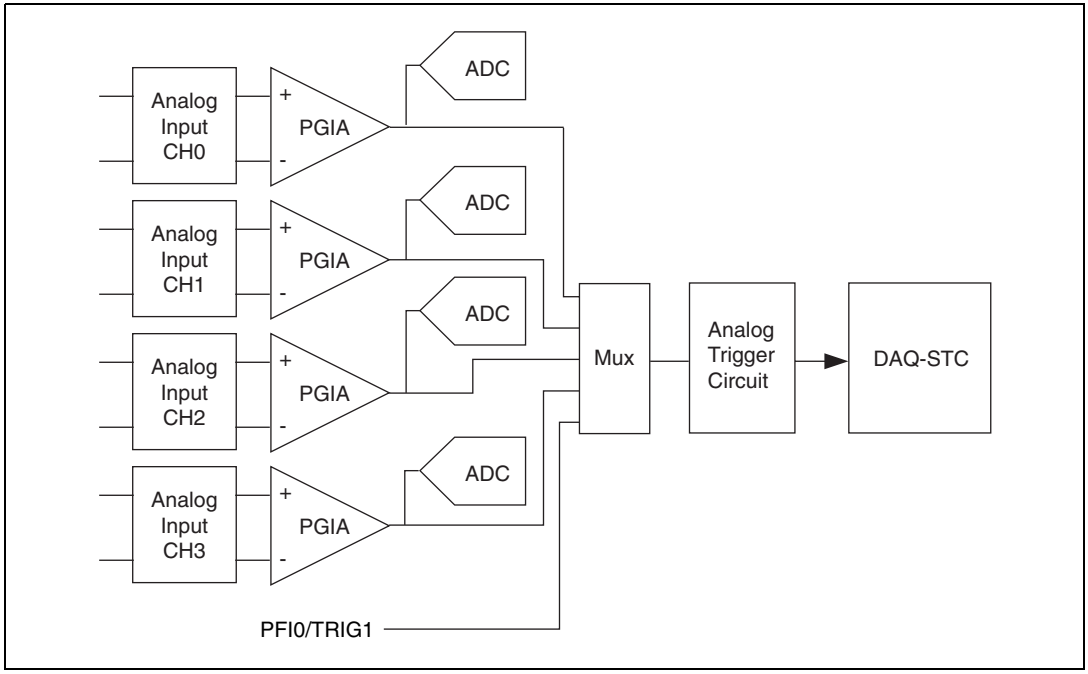


Figure 3-4. Analog Trigger Block Diagram for the PCI-6110

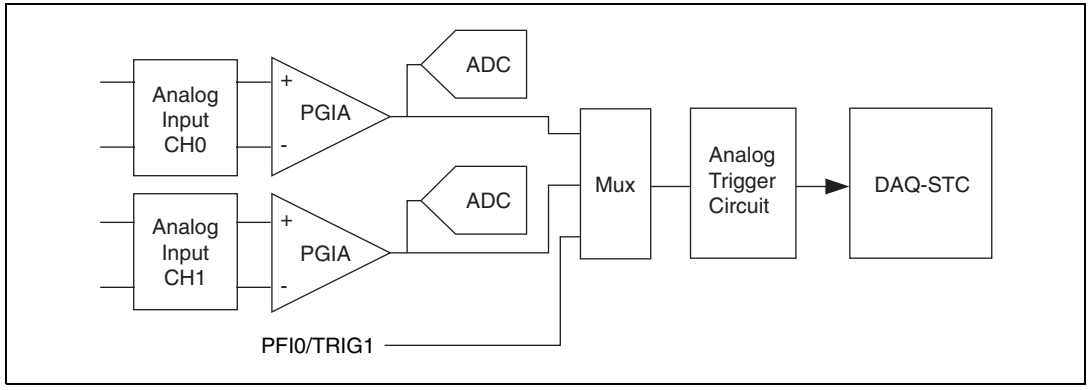


Figure 3-5. Analog Trigger Block Diagram for the PCI-6111

Five analog triggering modes are available, as shown in Figures 3-6 through 3-10. You can set **lowValue** and **highValue** independently in software.

In below-low-level analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, as shown in Figure 3-6. **HighValue** is unused.

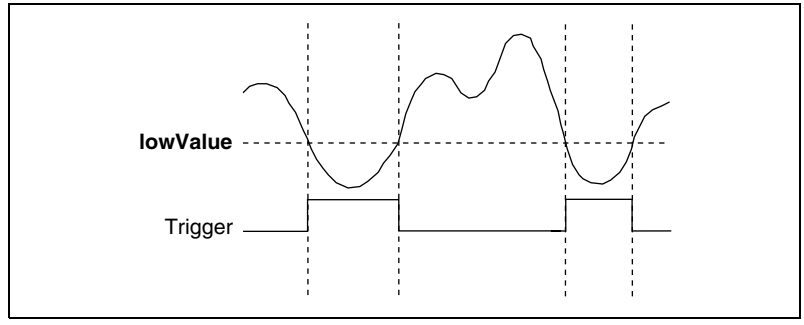


Figure 3-6. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, as shown in Figure 3-7. **LowValue** is unused.

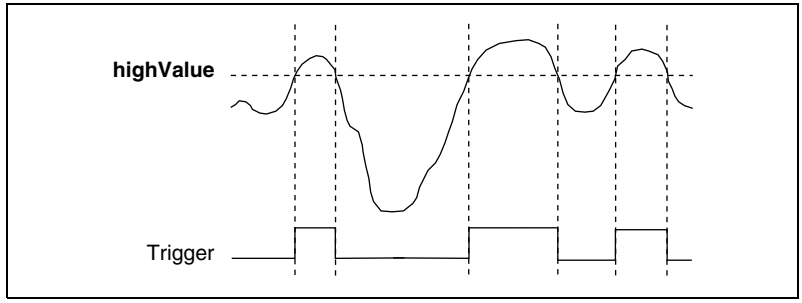


Figure 3-7. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, the trigger is generated when the signal value is between the **lowValue** and the **highValue**, as shown in Figure 3-8**.**

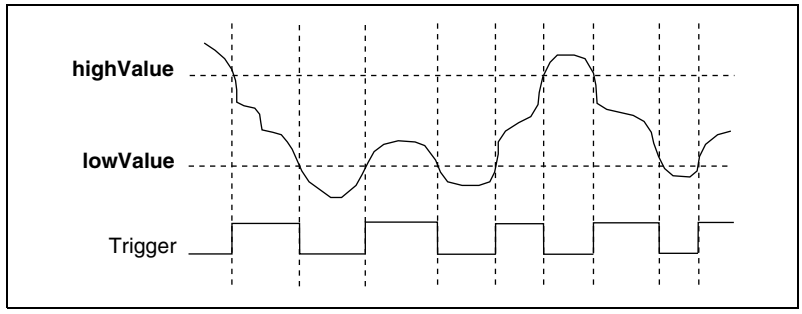


Figure 3-8. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**, as shown in Figure 3-9.

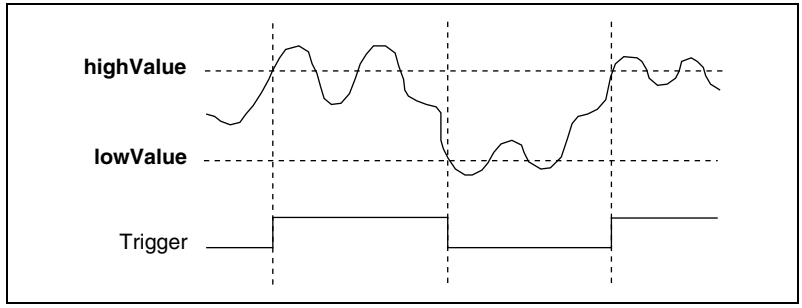


Figure 3-9. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue**, as shown in Figure 3-10**.**

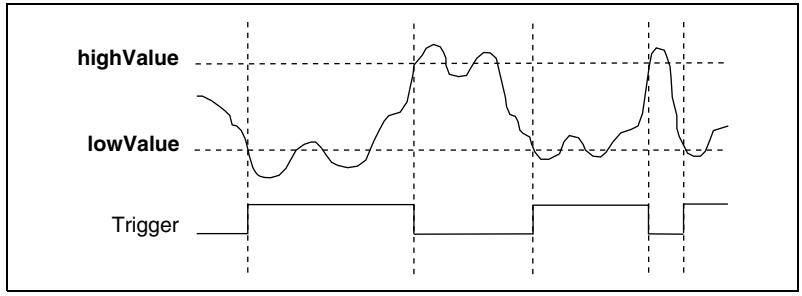


Figure 3-10. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the analog input signal and the user-defined trigger levels. This digital trigger can be used by any of the timing sections of the DAQ-STC, including the analog input, analog output, and general-purpose counter/timer sections. For example, the analog input section can be configured to acquire *n* scans after the analog input signal crosses a specific threshold. As another example, the analog output section can be configured to update its outputs whenever the analog input signal crosses a specific threshold.

Digital I/O

The 611*X* device contains eight lines of digital I/O for general-purpose use. You can individually software-configure each line for either input or output. At system startup and reset, the digital I/O ports are all high impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a very flexible interface for connecting timing signals to other devices or external circuitry. The 611*X* device uses the RTSI bus to interconnect timing signals between devices, and the Programmable Function Input (PFI) pins on the I/O connector to connect the device to external circuitry. These connections are designed to enable the 611*X* device to both control and be controlled by other devices and circuits.

There are a total of 13 timing signals internal to the DAQ-STC that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. For example, the signal routing multiplexer for controlling the CONVERT* signal is shown in Figure 3-11.

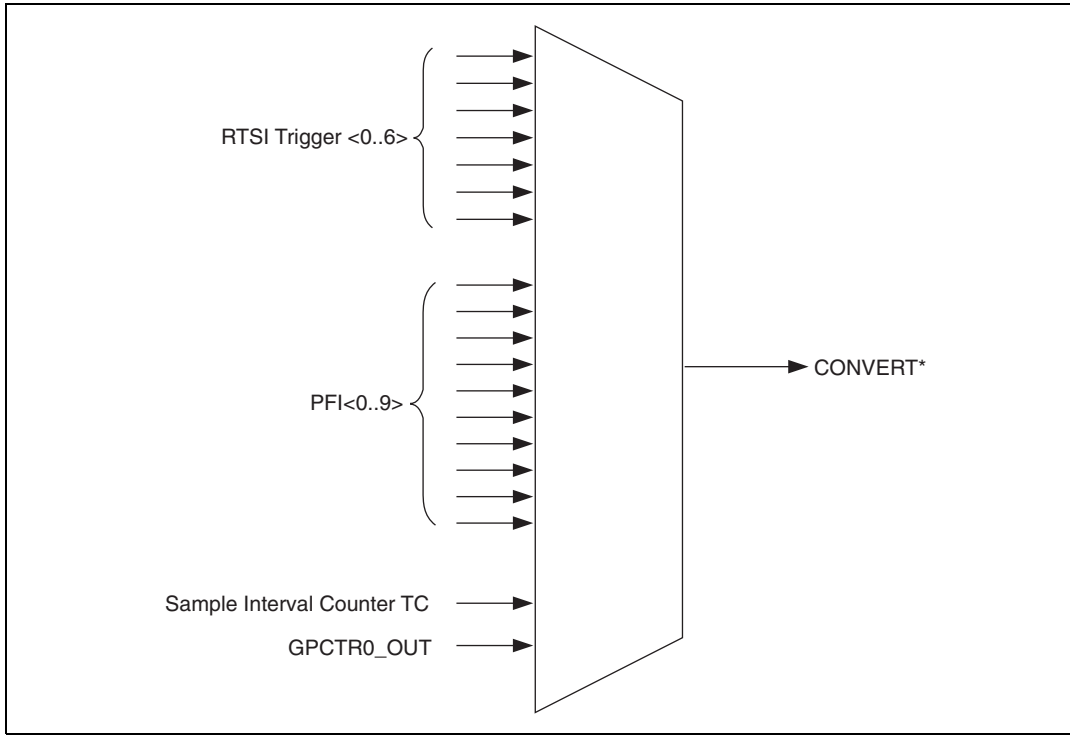


Figure 3-11. CONVERT* Signal Routing

This figure shows that CONVERT* can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section later in this chapter, and on the PFI pins, as indicated in Chapter 4, *Signal Connections*.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select one of the PFIs as the external source for a given timing signal. It is important to note that any of the PFIs can be used as an input by any of the timing signals and that multiple timing signals can use the same PFI simultaneously. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications. You can also individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

Device and RTSI Clocks

Many functions performed by the 611*X* device require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

The 611*X* device can use either its internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the device to use the internal timebase, you can also program the device to drive its internal timebase over the RTSI bus to another device that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the device as the primary frequency source. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal. This timebase is software selectable.

RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a very flexible interconnection scheme for the 611*X* device sharing the RTSI bus. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-12.

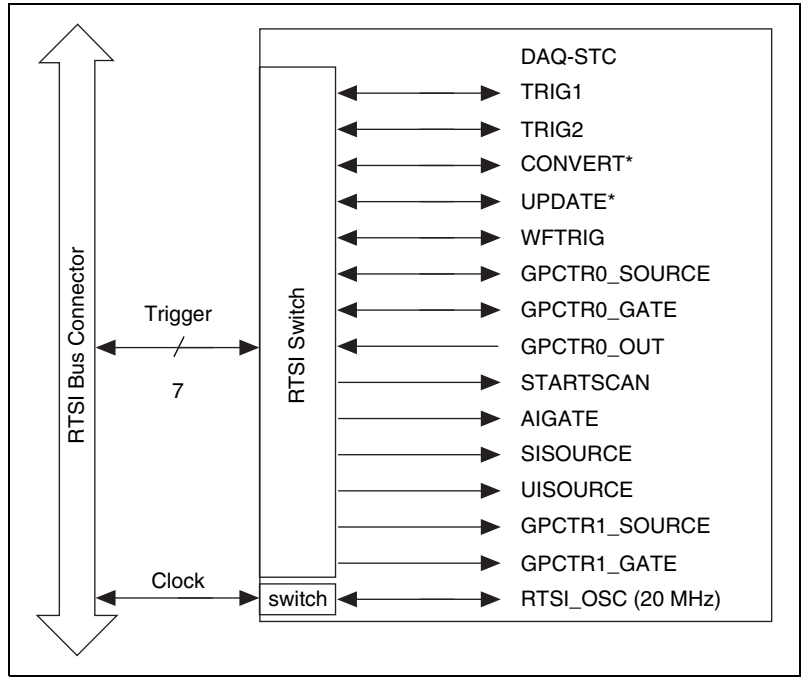


Figure 3-12. RTSI Bus Signal Connection

Refer to the *Timing Connections* section of Chapter 4, *Signal Connections*, for a description of the signals shown in Figure 3-12.

4

Signal Connections

This chapter describes how to make input and output signal connections to your 611*X* device via the device I/O connector.

The I/O connector for the 611*X* device has 68 pins that you can connect to 68-pin accessories with the SH6868EP shielded cable.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the 611*X* device. A signal description follows the connector pinouts.

Caution Connections that exceed any of the maximum ratings of input or output signals on the 611*X* device can damage the 611*X* device and the computer. Maximum input ratings for each signal are given in the *Protection* column of Table 4-2. National Instruments is *not* liable for any damages resulting from such signal connections.

ACH0–	34	68	ACH0+
ACH1+	33	67	ACH0GND
ACH1GND	32	66	ACH1–
ACH2–[1]	31	65	ACH2+[1]
ACH3+[1]	30	64	ACH2GND[1]
ACH3GND[1]	29	63	ACH3–[1]
NC	28	62	NC
NC	27	61	NC
NC	26	60	NC
NC	25	59	NC
NC	24	58	NC
NC	23	57	NC
DAC0OUT	22	56	NC
DAC1OUT	21	55	AOGND
NC	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

[1] NC on PCI-6111

Figure 4-1. I/O Connector Pin Assignment for the 611*X* Device

I/O Connector Signal Descriptions

Table 4-1. Signal Descriptions for I/O Connector Pins

Signal Name	Reference	Direction	Description
ACH <0..3> GND	—	—	Analog Input Channels 0 through 3 ground—These pins are the bias current return point for differential measurements. ACH <2..3> GND signals are no connects on the PCI-6111.
ACH<0..3> +	ACH <0..3> GND	Input	Analog Input Channels 0 through 3 (+)—These pins are routed to the (+) terminal of the respective channel's amplifier. ACH <2..3> + signals are no connects on the PCI-6111.
ACH<0..3> –	ACH <0..3> GND	Input	Analog Input Channels 0 through 3 (–)—These pins are routed to the (–) terminal of the respective channel's amplifier. ACH <2..3> – signals are no connects on the PCI-6111.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node.
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-resetting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.

Table 4-1. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
PFI0/TRIG1	DGND	Input	PFI0/Trigger 1—As an input, this is either one of the Programmable Function Inputs (PFIs) or the source for the hardware analog trigger. PFI signals are explained in the Timing Connections section later in this chapter. The hardware analog trigger is explained in the *Analog Trigger* section in Chapter 3, *Hardware Overview*.
		Output	As an output, this is the TRIG1 signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.
PFI1/TRIG2	DGND	Input	PFI1/Trigger 2—As an input, this is one of the PFIs.
		Output	As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is one of the PFIs.
		Output	As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is one of the PFIs.
		Output	As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated.

Table 4-1. Signal Descriptions for I/O Connector Pins (Continued)

Signal Name	Reference	Direction	Description
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is one of the PFIs.
		Output	As an output, this is the WFTRIG signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is one of the PFIs.
		Output	As an output, this is the STARTSCAN signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-2 shows the I/O signal summary for the 611*X* devices.

Table 4-2. I/O Signal Summary for the 611*X*

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..3> +	AI	1 MΩ in parallel with 100 pF[1] 1 MΩ in parallel with 10 pF[2]	42 V	—	—	—	—
ACH<0..3> –	AI	10 nF	42 V	—	—	—	±200 pA
ACH <0..3> GND	AI	—	—	—	—	—	—
DAC0OUT	AO	50 Ω	Short-circuit to ground	5 at 10	5 at -10	300 V/µs	—
DAC1OUT	AO	50 Ω	Short-circuit to ground	5 at 10	5 at -10	300 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1 A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} -0.4)	24 at 0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	AI DIO	10 kΩ	±35 V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	9 kΩ pu and 10 kΩ pd
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-2. I/O Signal Summary for the 611*X* (Continued)

Signal Name	Signal Type and Direction	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc}-0.4)	5 at 0.4	1.5	50 kΩ pu

[1] Applies to gain ≤ 1, impedance refers to ACH<0..3>–
[2]Applies to gain > 1, impedance refers to ACH<0..3>–

AI = Analog Input, DIO = Digital Input/Output, pu = pull-up, AO = Analog Output, DO = Digital Output, AI/DIO = Analog Input/Digital Input/Output

The tolerance on the 50 kΩ pull-up and pull-down resistors is very large. Actual value may range between 17 and 100 kΩ.

Analog Input Signal Connections

The analog input signals for the 611*X* device are ACH<0..3>+ and ACH<0..3>–. The ACH<0..3>+ signals are routed to the positive input of the PGIA, and signals connected to ACH<0..3>– are routed to the negative input of the PGIA.

Caution Exceeding the differential and common-mode input ranges distorts your input signals. Exceeding the maximum input voltage rating can damage the 611*X* device and the computer. National Instruments is *not* liable for any damages resulting from such signal connections. The maximum input voltage ratings are listed in the *Protection* column of Table 4-2.

With the different configurations, you can use the PGIA in different ways. Figure 4-2 shows a diagram of your 611*X* device PGIA.

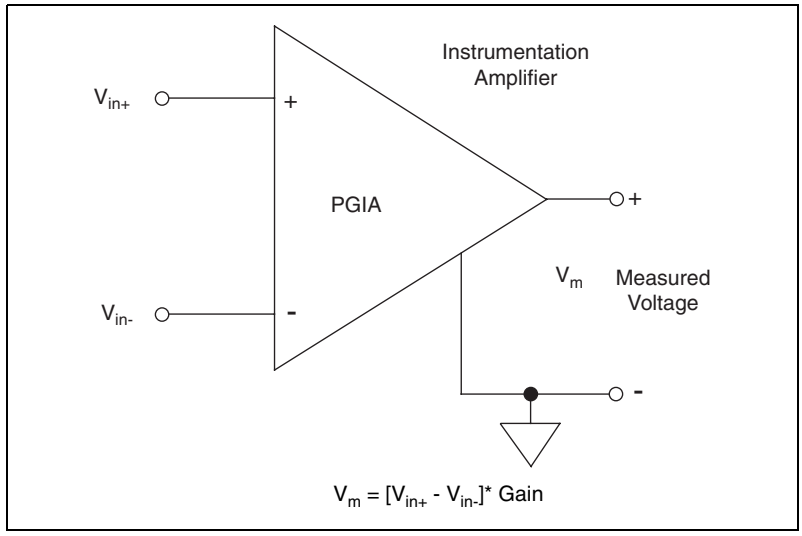


Figure 4-2. 611*X* Device PGIA

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the analog input signals connected to the 611*X* device. Signals are routed to the positive and negative inputs of the PGIA. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the device. The 611*X* device A/D converter (ADC) measures this output voltage when it performs A/D conversions.

Types of Signal Sources

When making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to the 611*X* device analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

A ground-referenced signal source is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the 611*X* device, assuming that the computer is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

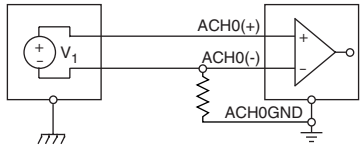
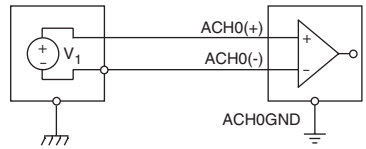
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

Differential Measurements

The following sections discuss the use of differential (DIFF) measurements and considerations for measuring both floating and ground-referenced signal sources.

Table 4-3 summarizes the recommended DIFF signal connections and includes input examples for both types of signal sources.

Table 4-3. Signal Source Types

DIFF Input Examples and Signal Source	Floating Signal Source (Not Connected to Building Ground)	Grounded Signal Source
Input Examples	• Ungrounded Thermocouples • Signal conditioning with isolated outputs • Battery devices	• Plug-in cards with nonisolated outputs
Differential (DIFF)	 See text for information on bias resistors.	

Differential Connection Considerations

A differential connection is one in which the 611*X* device analog input signal has its own reference signal or signal return path. The 611*X* channels are always configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

Each differential signal uses two inputs—one for the signal and one for its reference signal.

Differential signal connections reduce picked up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-3 shows how to connect a ground-referenced signal source to a channel on the 611*X* device.

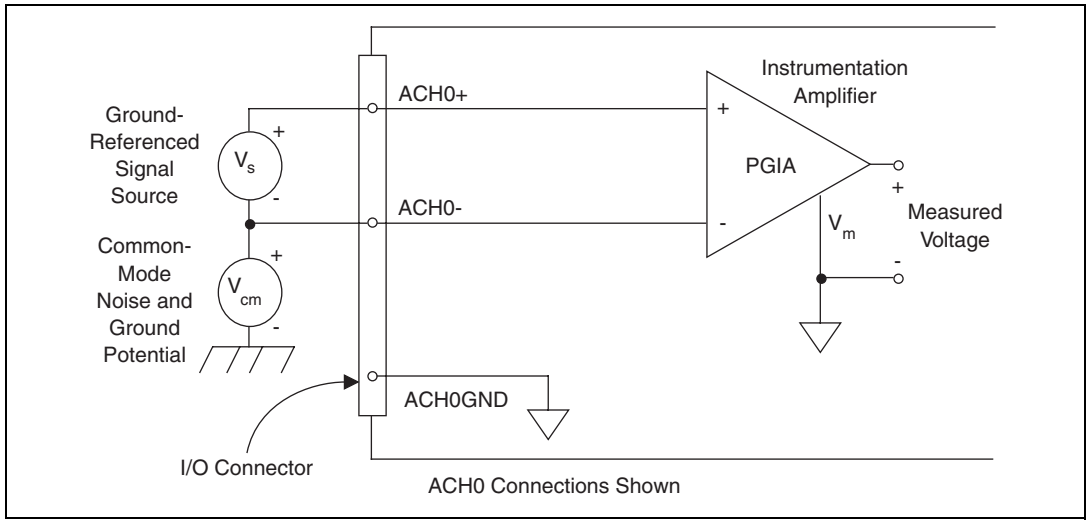


Figure 4-3. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the 611*X* device ground, shown as V_{cm} in Figure 4-3.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-4 shows how to connect a floating signal source to a channel on the 611*X* device.

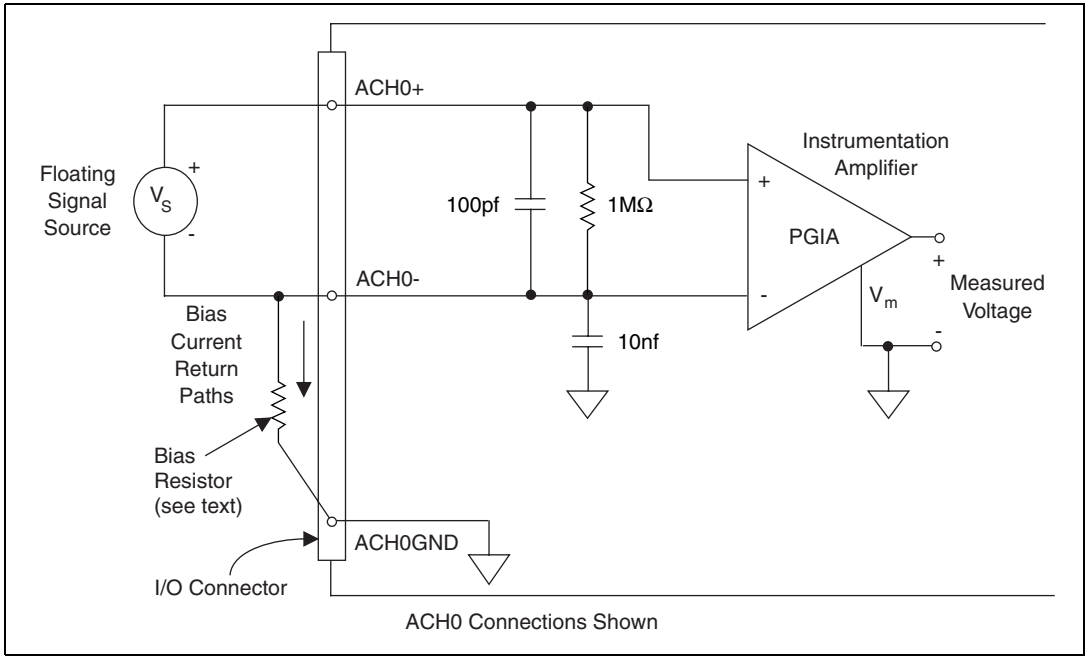


Figure 4-4. Differential Input Connections for Nonreferenced Signals

Figure 4-4 shows a bias resistor connected between ACH0 – and the floating signal source ground. If you do not use the resistor and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA, and the PGIA will saturate, causing erroneous readings. You must reference the source to the respective channel ground.

Common-Mode Signal Rejection Considerations

Figure 4-3 shows connections for signal sources that are already referenced to some ground point with respect to the 611*X* device. In this case, the PGIA can reject any voltage caused by ground potential differences between the signal source and the device. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the device. The PGIA can reject common-mode signals as long as V^+_{in} and V^-_{in} (input signals) are both within ±11 V of the channel ground, for gain ≥1. For gain <1, the input signals, for ACHO +, can be within ±42 V of the channel ground.

Analog Output Signal Connections

The analog output signals are DAC0OUT, DAC1OUT, and AOGND.

DAC0OUT is the voltage output signal for analog output channel 0. DAC1OUT is the voltage output signal for analog output channel 1.

AOGND is the ground reference signal for the analog output channels.

Figure 4-5 shows how to make analog output connections to the 611*X* device.

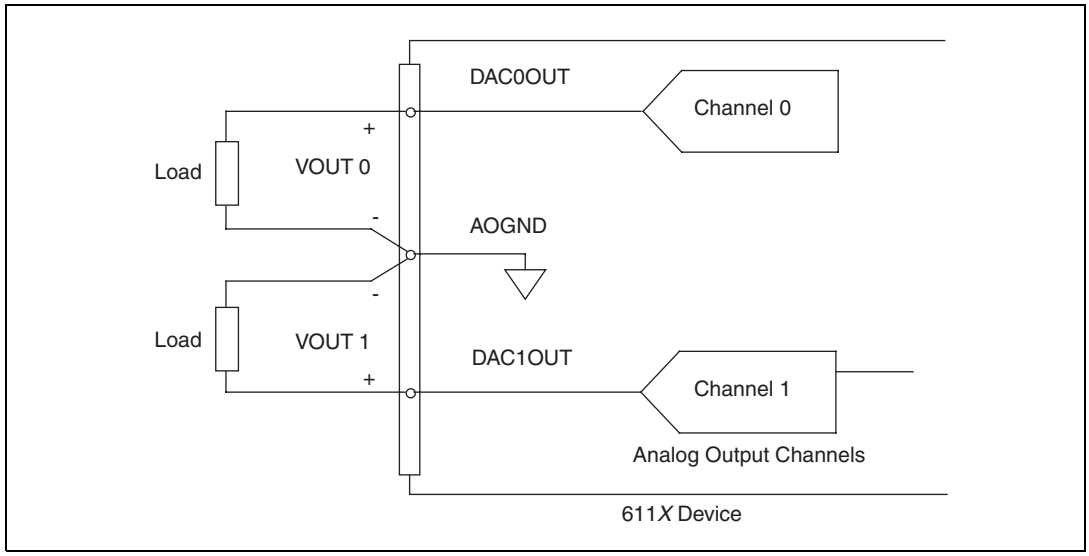


Figure 4-5. Analog Output Connections

Digital I/O Signal Connections

The digital I/O signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs.

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the 611*X* device and the computer. National Instruments is *not* liable for any damages resulting from such signal connections.

Figure 4-6 shows signal connections for three typical digital I/O applications.

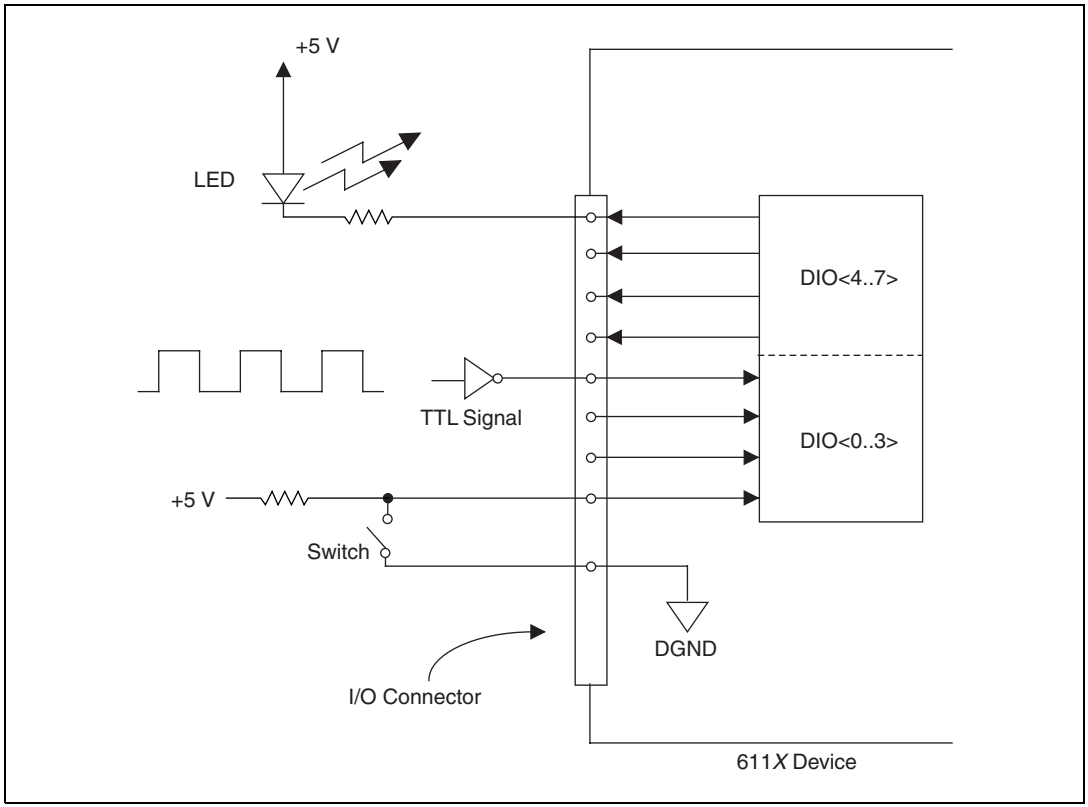


Figure 4-6. Digital I/O Connections

Figure 4-6 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the switch state shown in Figure 4-6. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 4-6.

Power Connections

Two pins on the I/O connector supply +5 V from the computer power supply via a self-resetting fuse. The fuse will reset automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry.

- Power rating +4.65 to +5.25 VDC at 1 A

Caution Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the 611*X* device or any other device. Doing so can damage the 611*X* device and the computer. National Instruments is *not* liable for damages resulting from such a connection.

Timing Connections

Caution Exceeding the maximum input voltage ratings, which are listed in Table 4-2, can damage the 611*X* device and the computer. National Instruments is *not* liable for any damages resulting from such signal connections.

All external control over the timing of the 611*X* device is routed through the 10 programmable function inputs labeled PFI0 through PFI9. These signals are explained in detail in the next section, *Programmable Function Input Connections*. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many DAQ, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any DAQ, waveform generation, and general-purpose timing signals.

The DAQ signals are explained in the *DAQ Timing Connections* section later in this chapter. The waveform generation signals are explained in the *Waveform Generation Timing Connections* section later in this chapter. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section later in this chapter.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-7, which shows how to connect an external TRIG1 source and an external CONVERT* source to two 611*X* device PFI pins.

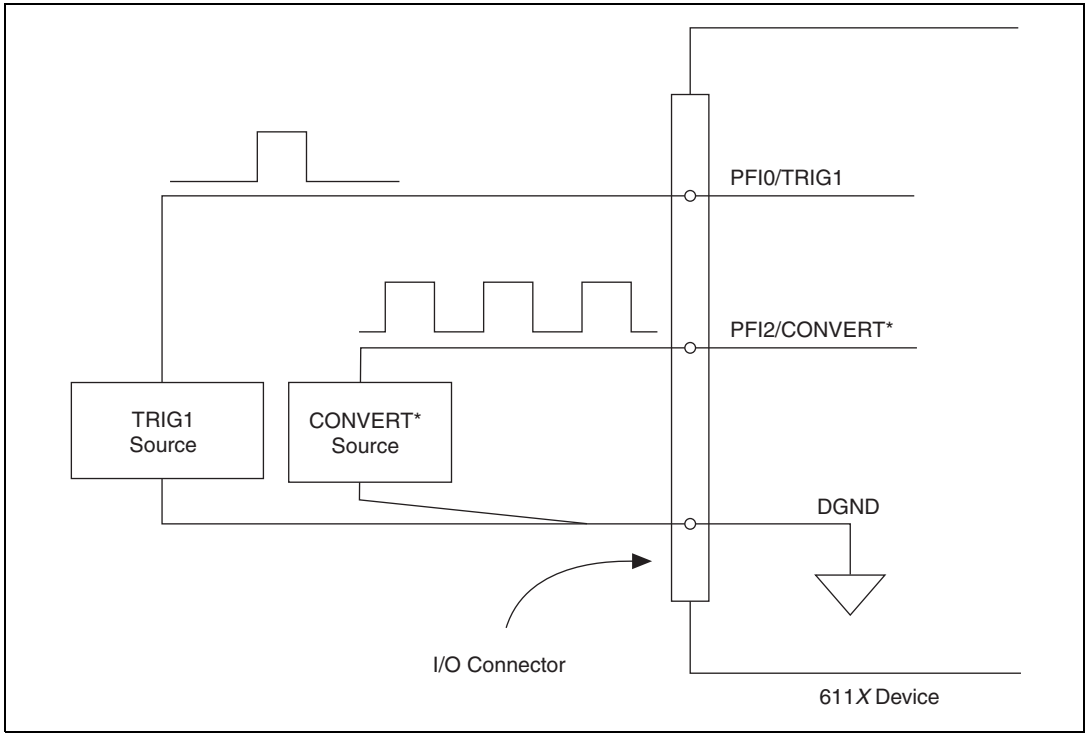


Figure 4-7. Timing I/O Connections

Programmable Function Input Connections

There are a total of 13 internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software-selectable from any of the PFIs when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the device I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. Be careful not to drive a PFI signal externally when it is configured as an output.

As an input, you can individually configure each PFI for edge or level detection and for polarity selection, as well. You can use the polarity selection for any of the 13 timing signals, but the edge or level detection will depend upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs themselves, but there may be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

DAQ Timing Connections

The DAQ timing signals are SCANCLK, EXTSTROBE*, TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, and SISOURCE.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-8. Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-9 shows a typical pretriggered DAQ sequence. The description for each signal shown in these figures is included later in this chapter.

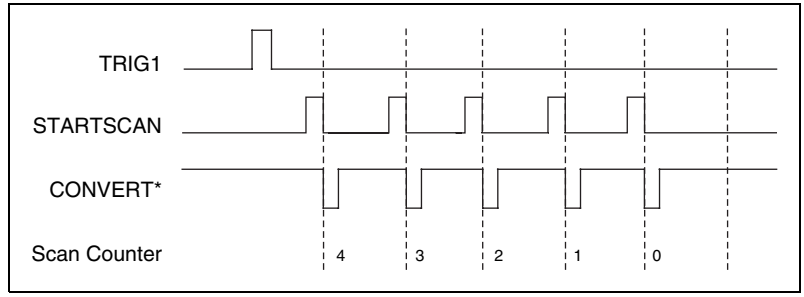


Figure 4-8. Typical Posttriggered Acquisition

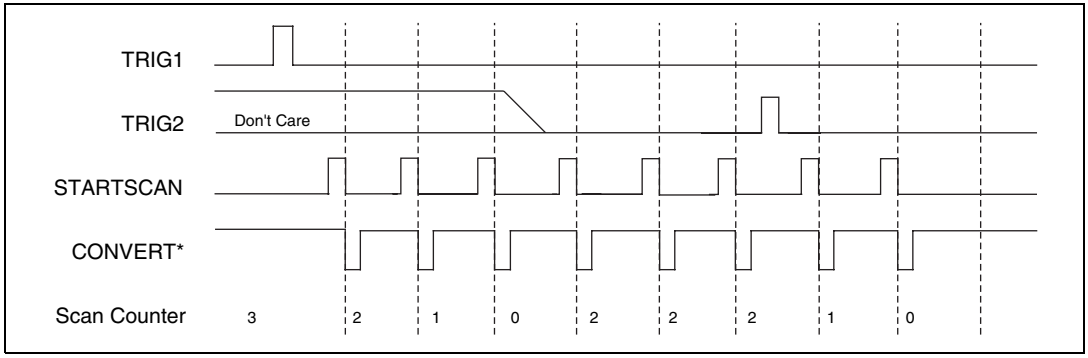


Figure 4-9. Typical Pretriggered Acquisition

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software-selectable but is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 450 ns pulse width and is software enabled. Figure 4-10 shows the timing for the SCANCLK signal.

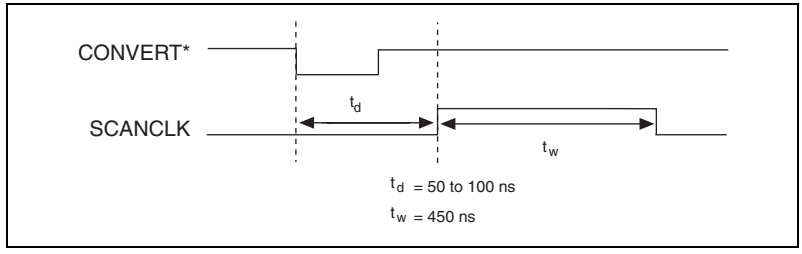


Figure 4-10. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode.

Figure 4-11 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

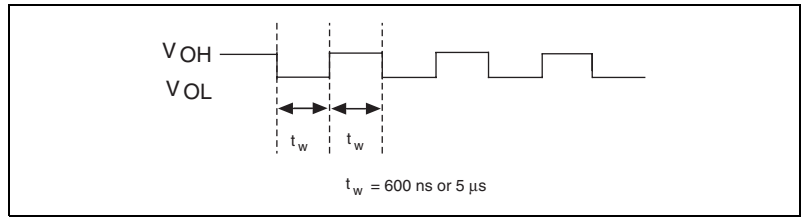


Figure 4-11. EXTSTROBE* Signal Timing

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-8 and 4-9 for the relationship of TRIG1 to the DAQ sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 signal starts the data acquisition sequence for both posttriggered and pretriggered acquisitions. The 611*X* supports analog triggering on the PFI0/TRIG1 pin. See Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, the TRIG1 signal reflects the action that initiates a DAQ sequence. This is true even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to tri-state at startup.

Figures 4-12 and 4-13 show the input and output timing requirements for the TRIG1 signal.

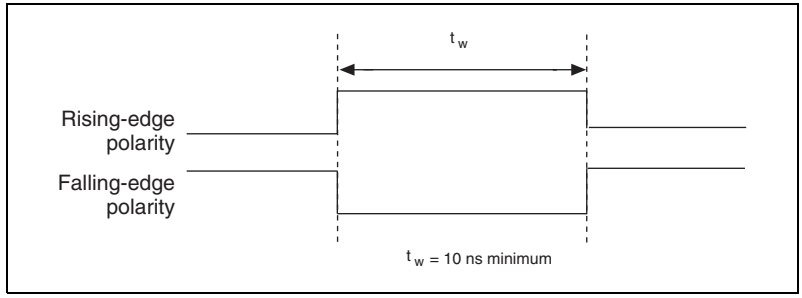


Figure 4-12. TRIG1 Input Signal Timing

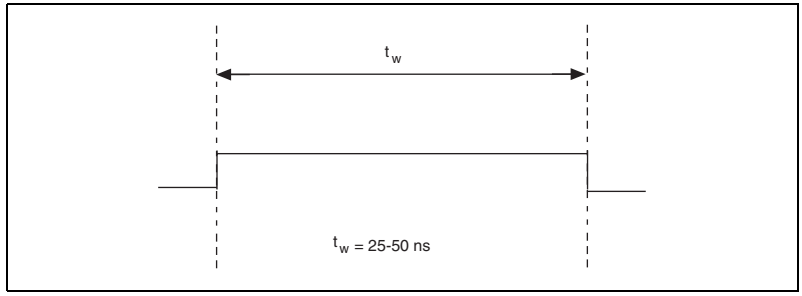


Figure 4-13. TRIG1 Output Signal Timing

The device also uses the TRIG1 signal to initiate pretriggered DAQ operations. In most pretriggered applications, the TRIG1 signal is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered DAQ operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin. Refer to Figure 4-9 for the relationship of TRIG2 to the DAQ sequence.

As an input, the TRIG2 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG2 signal initiates the posttriggered phase of a pretriggered acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans

before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The device ignores the TRIG2 signal if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the device will acquire a fixed number of scans and the acquisition will stop. This mode acquires data both before and after receiving TRIG2.

As an output, the TRIG2 signal reflects the posttrigger in a pretriggered acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The TRIG2 signal is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to tri-state at startup.

Figures 4-14 and 4-15 show the input and output timing requirements for the TRIG2 signal.

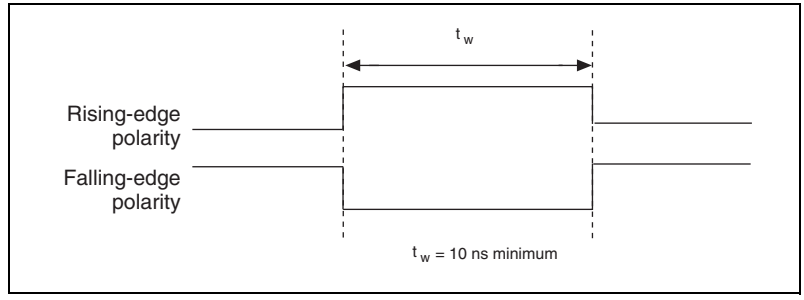


Figure 4-14. TRIG2 Input Signal Timing

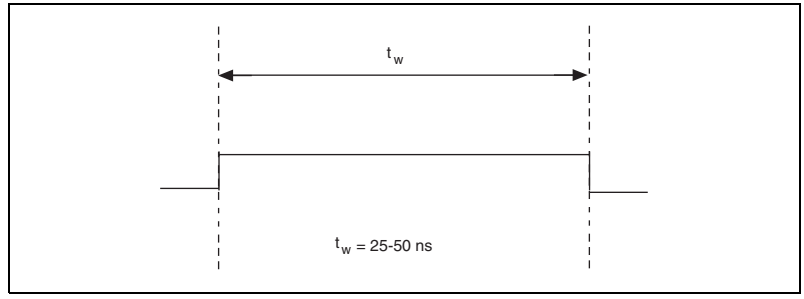


Figure 4-15. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin. Refer to Figures 4-8 and 4-9 for the relationship of STARTSCAN to the DAQ sequence.

As an input, the STARTSCAN signal is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval counter starts if you select internally triggered CONVERT*.

As an output, the STARTSCAN signal reflects the actual start pulse that initiates a scan. This is true even if the starts are being externally triggered by another PFI. You have two output options. The first is an active high pulse with a pulse width of 25 to 50 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN will be deasserted t_{off} after the last conversion in the scan is initiated. This output is set to tri-state at startup.

Figures 4-16 and 4-17 show the input and output timing requirements for the STARTSCAN signal.

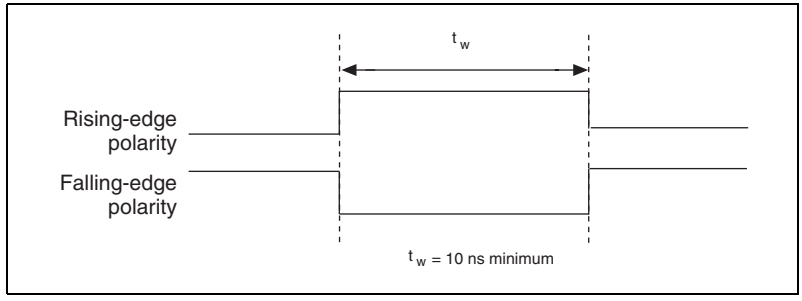


Figure 4-16. STARTSCAN Input Signal Timing

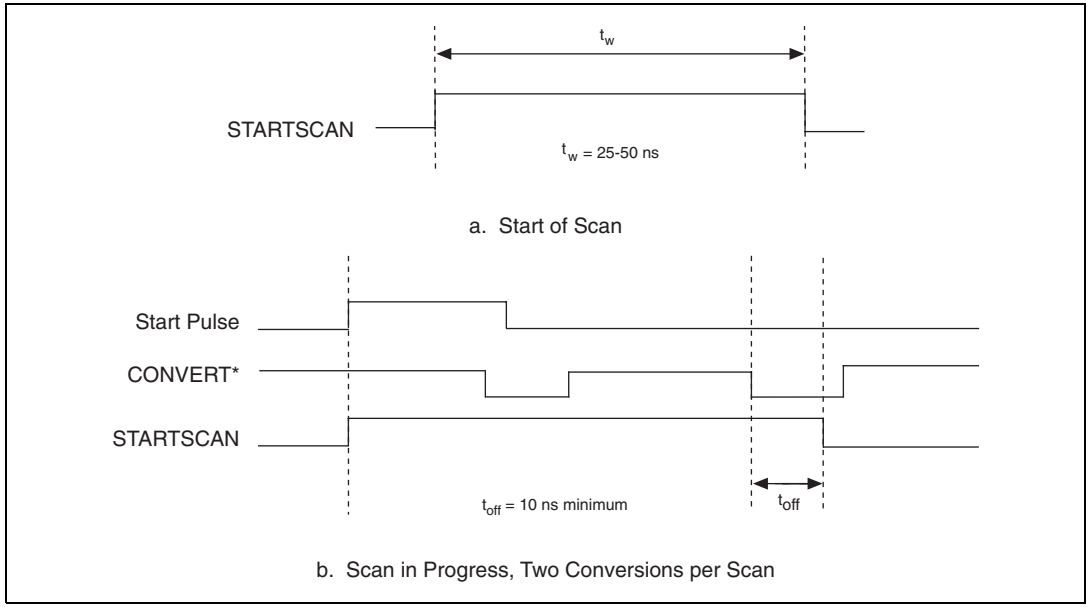


Figure 4-17. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the device generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* appears when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN generates a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on the 611*X* device internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-8 and 4-9 for the relationship of STARTSCAN to the DAQ sequence.

As an input, the CONVERT* signal is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of the CONVERT* signal initiates an A/D conversion.

As an output, the CONVERT* signal reflects the actual convert pulse that is connected to the ADC. This is true even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-18 and 4-19 show the input and output timing requirements for the CONVERT* signal.

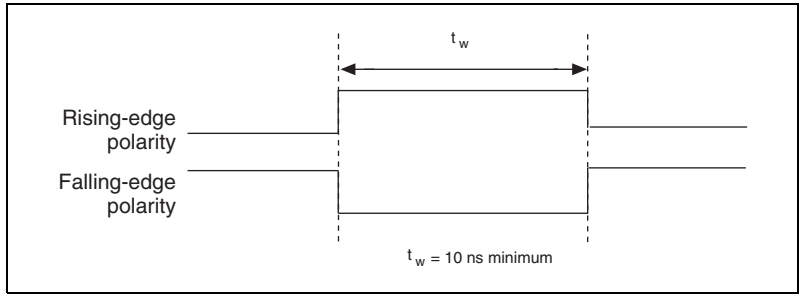


Figure 4-18. CONVERT* Input Signal Timing

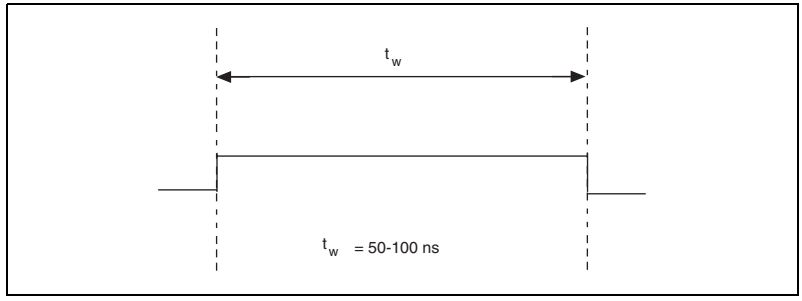


Figure 4-19. CONVERT* Output Signal Timing

The ADC switches to hold mode within 20 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next.

The sample interval counter on the 611*X* device normally generates the CONVERT* signal unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in preparation for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a DAQ sequence. Scans occurring within a DAQ sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a DAQ sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur. In the edge-detection mode, the first active edge disables the STARTSCAN signal, and the second active edge enables STARTSCAN.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for the SISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates the SISOURCE signal unless you select some external source. Figure 4-20 shows the timing requirements for the SISOURCE signal.

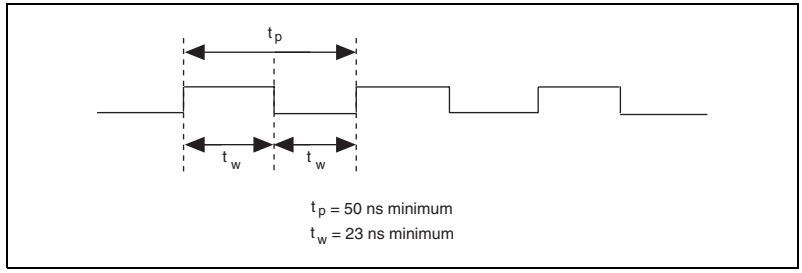


Figure 4-20. SISOURCE Signal Timing

Waveform Generation Timing Connections

The analog group defined for the 611*X* device is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, the WFTRIG signal is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of the WFTRIG signal starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, the WFTRIG signal reflects the trigger that initiates waveform generation. This is true even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 25 to 50 ns. This output is set to tri-state at startup.

Figures 4-21 and 4-22 show the input and output timing requirements for the WFTRIG signal.

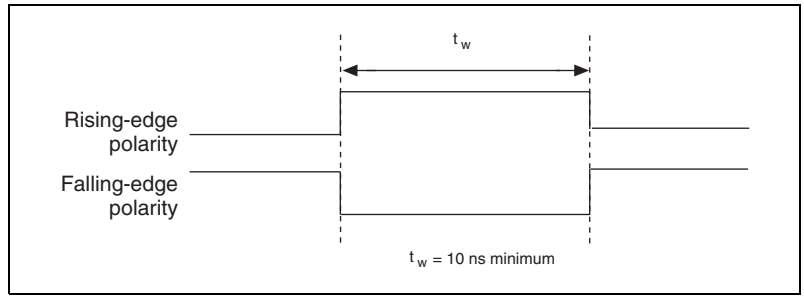


Figure 4-21. WFTRIG Input Signal Timing

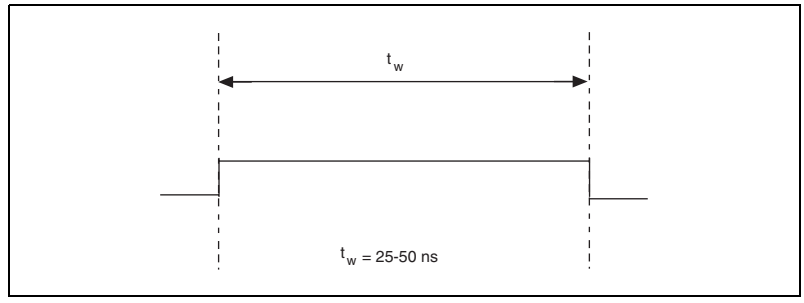


Figure 4-22. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, the UPDATE* signal is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of the UPDATE* signal updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, the UPDATE* signal reflects the actual update pulse that is connected to the DACs. This is true even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 75 ns. This output is set to tri-state at startup.

Figures 4-23 and 4-24 show the input and output timing requirements for the UPDATE* signal.

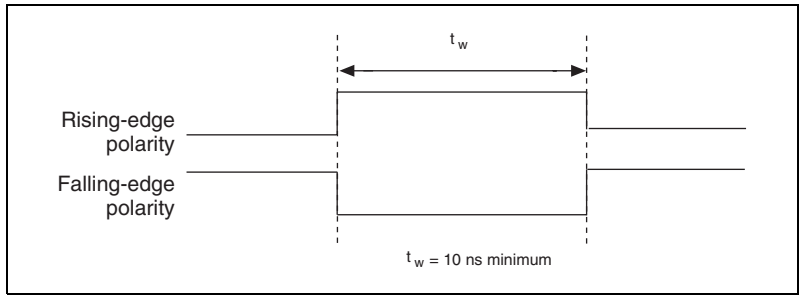


Figure 4-23. UPDATE* Input Signal Timing

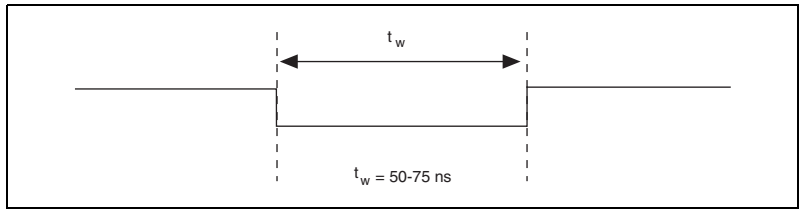


Figure 4-24. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The UI counter for the 611*X* device normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

Figure 4-25 shows the timing requirements for the UISOURCE signal.

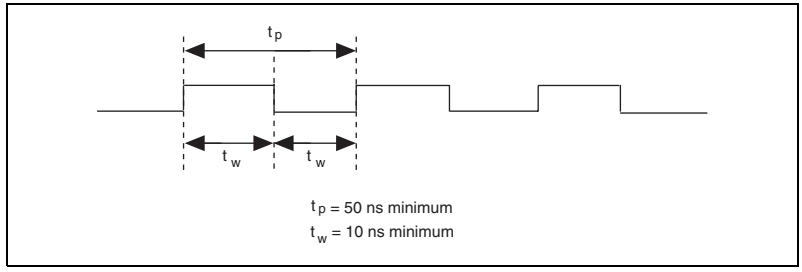


Figure 4-25. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR0_SOURCE signal reflects the actual clock connected to general-purpose counter 0. This is true even if another PFI is externally inputting the source clock. This output is set to tri-state at startup.

Figure 4-26 shows the timing requirements for the GPCTR0_SOURCE signal.

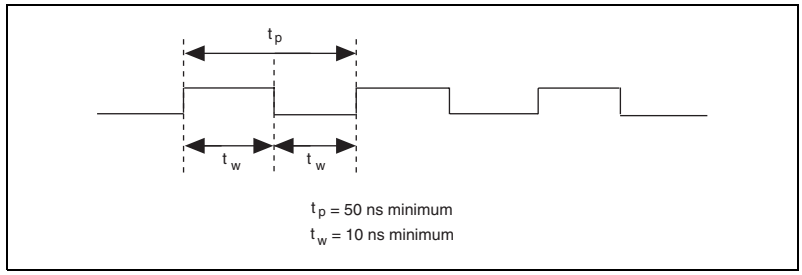


Figure 4-26. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-27 shows the timing requirements for the GPCTR0_GATE signal.

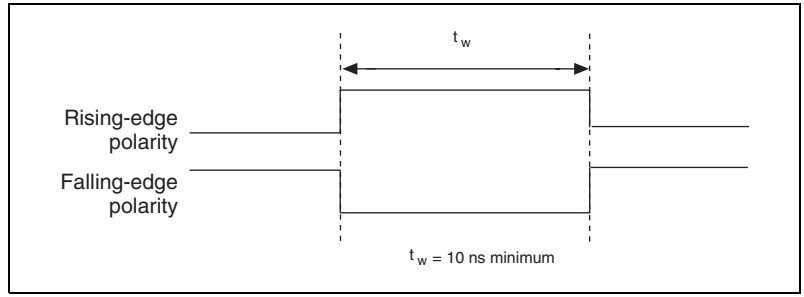


Figure 4-27. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-28 shows the timing of the GPCTR0_OUT signal.

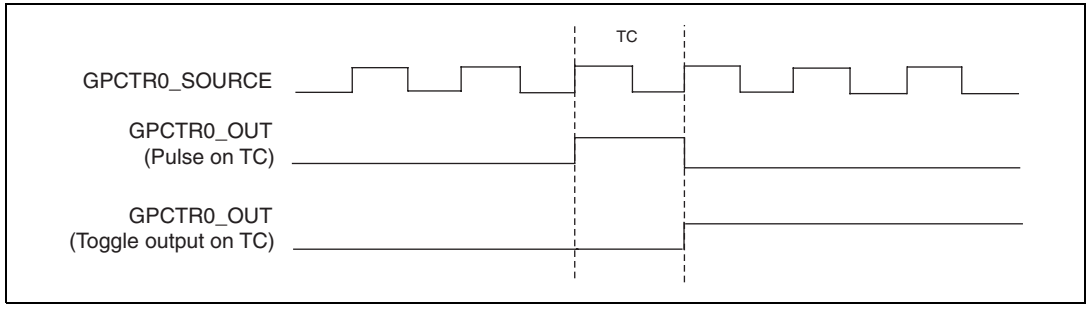


Figure 4-28. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 will count down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.
As an input, the GPCTR1_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1. This is true even if the source clock is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-29 shows the timing requirements for the GPCTR1_SOURCE signal.

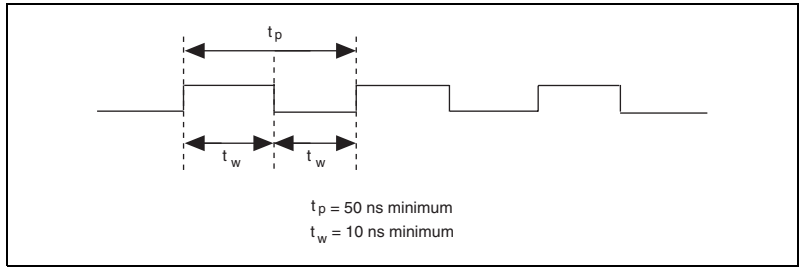


Figure 4-29. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-30 shows the timing requirements for the GPCTR1_GATE signal.

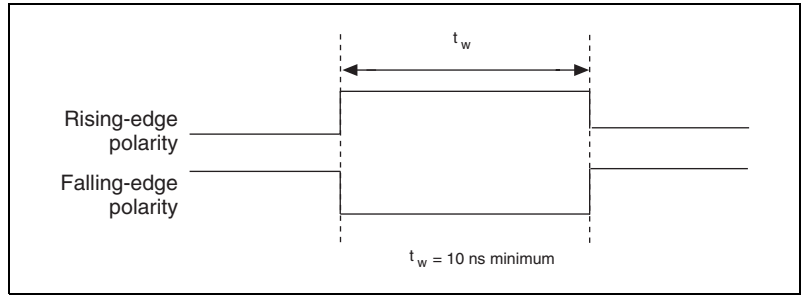


Figure 4-30. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC device general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-31 shows the timing requirements for the GPCTR1_OUT signal.

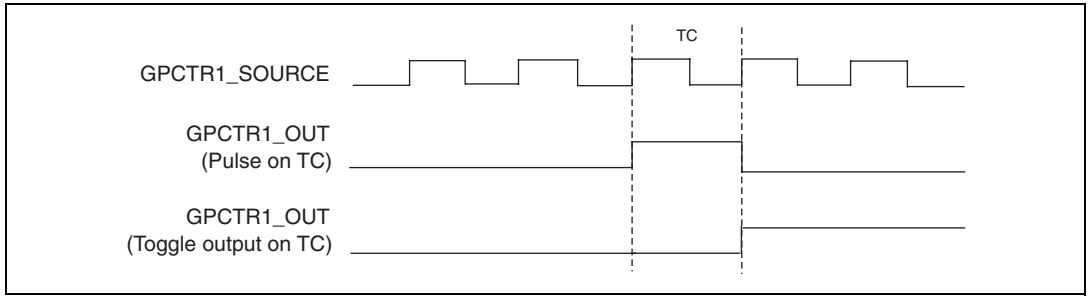
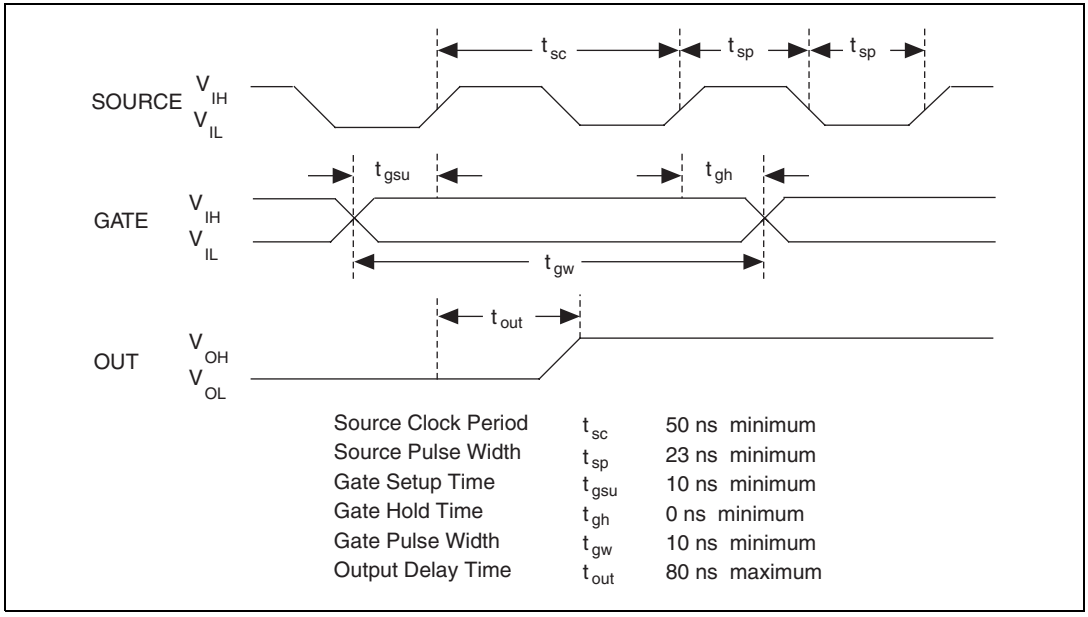


Figure 4-31. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-32 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the 611*X* device OUT output signals.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-32. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-32 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on the 611*X* device. Figure 4-32 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-32.

The gate signal is not required to be held after the active edge of the source signal.

If you use an internal timebase clock, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the 611*X* device. Figure 4-32 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The frequency generator for the 611*X* device outputs the FREQ_OUT pin. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software-selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software selectable. This output is set to tri-state at startup.

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with the 611*X* device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to analog input signal routing to the device, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential analog input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect analog input signals to the device. With this type of wire, the signals attached to the ACH+ and ACH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling

through areas with large magnetic fields or high electromagnetic interference.

- Route signals to the device carefully. Keep cabling away from noise sources. The most common noise source in a PCI data acquisition system is the video monitor. Separate the monitor from the analog signals as much as possible.
- The following recommendations apply for all signal connections to the 611*X* device:
- Separate the 611*X* device signal lines from high-current or high-voltage lines. These lines can induce currents in or voltages on the 611*X* device signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the application note, *Field Wiring and Noise Consideration for Analog Signals,* available from National Instruments.

5

Calibration

This chapter discusses the calibration procedures for your 611*X* device. If you are using the NI-DAQ device driver, that software includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the 611*X* device, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of device calibration is required for all but the most forgiving applications. If you do not calibrate your device, your signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you and described in this chapter. The first level is the fastest, easiest, and least accurate; whereas, the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

The 611*X* device is factory calibrated before shipment at approximately 25 °C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the device is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ software determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the device measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the device is installed in the environment in which it will be used.

Self-Calibration

The 611*X* device can measure and correct for almost all of its calibration-related errors without any external signal connections. Your National Instruments software provides a self-calibration method. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. Initiate self-calibration to minimize the effects of any offset, gain, and linearity drifts, particularly those due to warmup.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

The 611*X* device has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using your device at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate your device.

An external calibration refers to calibrating your device with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate your device by calling the NI-DAQ calibration function.

To externally calibrate your device, be sure to use a very accurate external reference. The reference should be several times more accurate than the device itself. For example, to calibrate a 16-bit device, the external reference should be at least ±0.001% (±10 ppm) accurate.

A

Specifications

This appendix lists the specifications of your 611*X* device. These specifications are typical at 25 °C unless otherwise noted.

Analog Input

Input Characteristics

Number of channels

PCI-6110 ..... 4 differential

PCI-6111 ..... 2 differential

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate ..... 5 MS/s

Min sampling rate ..... 1 kS/s

Analog input characteristics

Input Range	Gain Error[1]	Offset Error	SFDR[2]	CMRR[3]	System Noise[4]
±50 V	0.50%	10 mV	70 dB	32 dB	0.5
±20 V	0.50%	10 mV	70 dB	35 dB	0.5
±10 V	0.10%	0.8 mV	75 dB	50 dB	0.5
±5 V	0.05%	0.5 mV	75 dB	56 dB	0.5
±2 V	0.05%	0.28 mV	75 dB	62 dB	0.5
±1 V	0.05%	0.20 mV	75 dB	67 dB	0.5
±500 mV	0.05%	0.15 mV	75 dB	70 dB	0.6
±200 mV	0.05%	0.10 mV	75 dB	72 dB	1.0

[1] Relative to reading, max
[2] All input ranges, DC to 100 kHz
[3] All input ranges, DC to 60 Hz
[4] LSB_{rms}, not including quantization

Input coupling.....DC/AC

Max working voltage for all analog input channels

+ input.....Should remain within ±11 V for ranges ≥ ±10 V; should remain within ±42 V for ranges < ±10 V

– input.....Should remain within ±11 V

Overvoltage protection .....±42 V

Inputs protected

+ input.....all channels

– input.....all channels

FIFO buffer size.....8,192 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Scatter-gather

Accuracy Information

See following table

PCI-6110/6111 Accuracy Information

Nominal Range (V)	Absolute Accuracy							Relative Accuracy	
	% of Reading			Offset	Noise + Quantization (mV)		Temp Drift	Resolution (mV)	
Full Scale	24 Hours	90 Days	1 Year	(mV)	Single Pt.	Averaged	(%/° C)	Theoretical	Averaged
±50	0.51%	0.51%	0.51%	35 mV	51 mV	4.4 mV	0.0005%	24 mV	5.8 mV
±20	0.51%	0.51%	0.51%	20 mV	20 mV	1.8 mV	0.0005%	9.8 mV	2.3 mV
±10	0.11%	0.11%	0.11%	5.7 mV	10 mV	0.88 mV	0.0005%	4.9 mV	1.2 mV
±5	0.057%	0.058%	0.059%	3 mV	5.1 mV	0.44 mV	0.0005%	2.4 mV	0.58 mV
±2	0.057%	0.058%	0.059%	1.3 mV	2 mV	0.18 mV	0.0005%	0.98 mV	0.23 mV
±1	0.057%	0.058%	0.059%	0.7 mV	1 mV	0.088 mV	0.0005%	0.49 mV	0.12 mV
±0.5	0.057%	0.058%	0.059%	0.4 mV	0.67 mV	0.059 mV	0.0005%	0.24 mV	0.077 mV
±0.2	0.057%	0.058%	0.059%	0.2 mV	0.39 mV	0.035 mV	0.0005%	0.098 mV	0.046 mV

Note: Accuracies are valid for measurements following an internal calibration. Averaged numbers assume dithering and averaging of 100 single-channel readings.

Measurement accuracies are listed for operational temperatures within ±1° C of internal calibration temperature and ±10° C of external or factory calibration temperature. One year calibration interval recommended.

Transfer Characteristics

INL.....±0.5 LSB typ, ±1 LSB max

DNL.....±0.3 LSB typ, ±0.75 LSB max

Spurious free dynamic range (SFDR) ....See table, analog input characteristics

Effective number of bits (ENOB).....11.0 bits, DC to 100 kHz

Offset error .....See table, analog input characteristics

Amplifier Characteristics

Input impedance .....1 MΩ in parallel with 100 pF

Input bias current.....±200 pA

Input offset current .....±100 pA

CMRR.....See table, analog input characteristics

Dynamic Characteristics

Interchannel skew .....1 ns typ
f_{in} = 100 kHz
input range = ±10 V

Bandwidth (0.5 to –3 dB)

Input range > ±0.2 V .....5 MHz

Input range = ±0.2 V .....4 MHz

System noise .....See table, analog input characteristics

Crosstalk .....–80 dB, DC to 100 kHz

Stability

Recommended warm-up time ..... 15 min.

Offset temperature coefficient

- Pregain ..... ±5 µV/°C
- Postgain ..... ±50 µV/°C

Gain temperature coefficient ..... ±20 ppm/°C

Onboard calibration reference

- Level ..... 5.000 V (±2.5 mV) (actual value stored in EEPROM)
- Temperature coefficient ..... ±0.6 ppm/°C max
- Long-term stability ..... ±6 ppm/$\sqrt{1,000\ h}$

Analog Output

Output Characteristics

Number of channels ..... 2 voltage

Resolution ..... 16 bits, 1 in 65,536

Max update rate

- 1 channel ..... 4 MS/s, system dependent
- 2 channel ..... 2.5 MS/s, system dependent

FIFO buffer size ..... 2,048 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter gather

Transfer Characteristics

Relative accuracy (INL) ..... ±4 LSB typ, ±8 LSB max

DNL ..... ±2 LSB typ, ±8 LSB max

Offset error ..... ±5.0 mV max

Gain error
(relative to internal reference) ..... ±0.1% of output range max

Voltage Output

Ranges .....±10 V

Output coupling .....DC

Output impedance.....50 Ω ±5%

Current drive.....±5 mA min

Output stability .....Any passive load

Protection.....Short-circuit to ground

Power-on state .....0 V

Dynamic Characteristics

Slew rate .....300 V/µs

Noise.....1 mV_{rms}, DC to 5 MHz

Spurious free dynamic range .....75 dB, DC to 10 kHz

Stability

Offset temperature coefficient .....±500 µV/°C

Gain temperature coefficient

- Internal reference.....±50 ppm/°C
- External reference.....±25 ppm/°C

Onboard calibration reference

- Level.....5.000 V (±2.5 mV) (actual value stored in EEPROM)
- Temperature coefficient.....±0.6 ppm/°C max
- Long-term stability .....±6 ppm/$\sqrt{1,000\ h}$

Digital I/O

Number of channels.....8 input/output

Compatibility .....TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0.0 V	0.8 V
Input high voltage	2.0 V	5.0 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state ..... Input (High-Z)

Data transfers ..... Programmed I/O

Timing I/O

Number of channels ..... 2 up/down counter/timers, 1 frequency scaler

Resolution

- Counter/timers ..... 24 bits
- Frequency scaler ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

- Counter/timers ..... 20 MHz, 100 kHz
- Frequency scaler ..... 10 MHz, 100 kHz

Base clock accuracy ..... ±0.01%

Max source frequency ..... 20 MHz

Min source pulse duration ..... 10 ns, edge-detect mode

Min gate pulse duration ..... 10 ns, edge-detect mode

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Scatter-gather

Triggers

Analog Trigger

Source

PCI-6110.....All analog input channels, external trigger (PFI0/TRIG1)

PCI-6111.....All analog input channels, external trigger (PFI0/TRIG1)

Level ..... ± full-scale, internal; ±10 V, external

Slope .....Positive or negative (software selectable)

Resolution .....8 bits, 1 in 256

Hysteresis.....Programmable

Bandwidth .....(–3 dB) 5 MHz internal/external

External input (PFI0/TRIG1)

Impedance.....10 kΩ

Coupling .....AC/DC

Protection.....–0.5 V to (V_{cc} + 0.5) V when configured as a digital signal, ±35 V when configured as an analog trigger signal or disabled, ±35 V powered off

Digital Trigger

Compatibility .....TTL

Response .....Rising or falling edge

Pulse width .....10 ns min

RTSI

Trigger Lines 7

Bus Interface

Type ..... Master, slave

Power Requirement

+5 VDC (±5%)

PCI-6110 ..... 2.5 A

PCI-6111 ..... 2.0 A

Power available at I/O connector ..... +4.65 to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors) ..... 31.2 by 10.6 cm
(12.3 by 4.2 in)

I/O connector ..... 68-pin male SCSI-II type

Environment

Operating temperature ..... 0 to 45 °C

Storage temperature ..... –20 to 70 °C

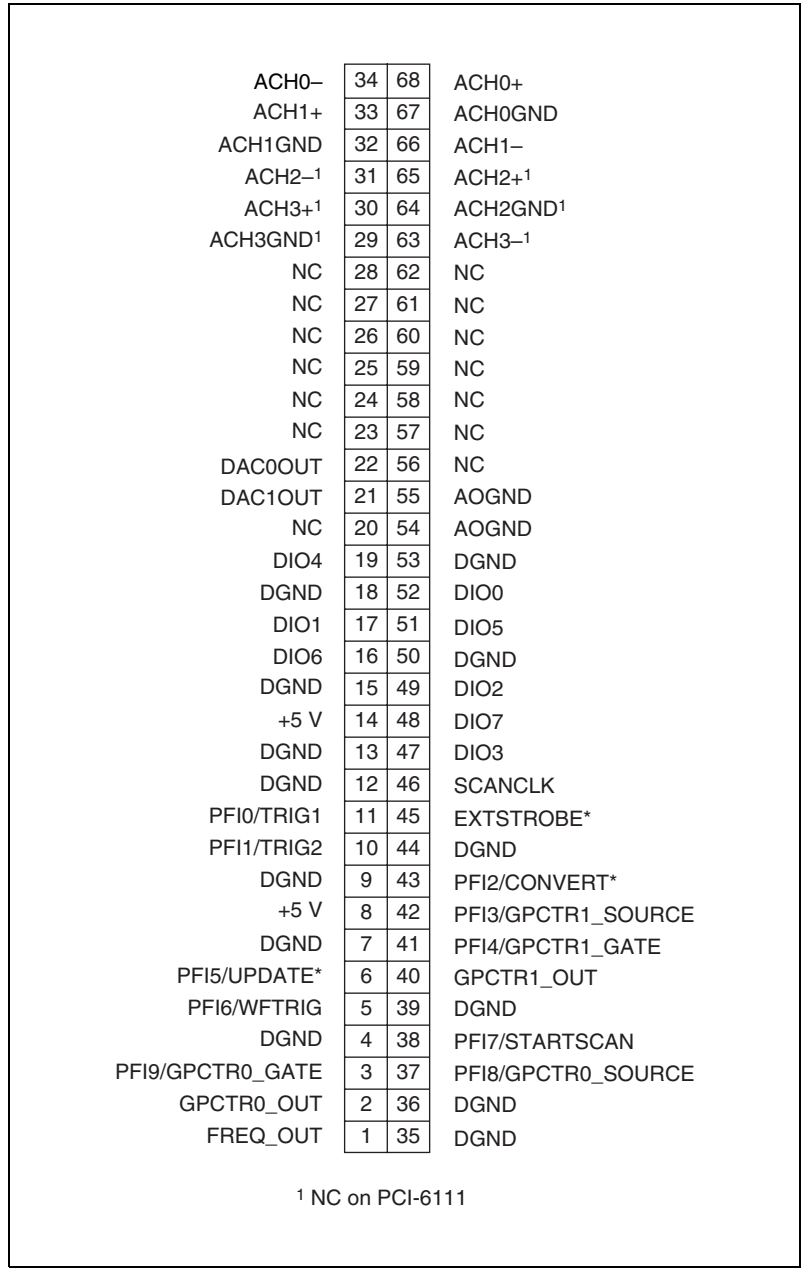
Relative humidity ..... 5 to 90% noncondensing

B

Cable Connector Descriptions

This appendix describes the cable connectors on your 611*X* device.

Figure B-1 shows the pin assignments for the 68-pin 611*X* connector. This connector is available when you use the SH6868EP cable assemblies with the 611*X* device.



ACH0–	34	68	ACH0+
ACH1+	33	67	ACH0GND
ACH1GND	32	66	ACH1–
ACH2–[1]	31	65	ACH2+[1]
ACH3+[1]	30	64	ACH2GND[1]
ACH3GND[1]	29	63	ACH3–[1]
NC	28	62	NC
NC	27	61	NC
NC	26	60	NC
NC	25	59	NC
NC	24	58	NC
NC	23	57	NC
DAC0OUT	22	56	NC
DAC1OUT	21	55	AOGND
NC	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

[1] NC on PCI-6111

Figure B-1. 68-Pin 611*X* Connector Pin Assignments

C

Common Questions

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of your 611*X* device.

General Information

What is the 611*X* device?

The 611*X* device is a switchless and jumperless enhanced MIO device that uses the DAQ-STC for timing.

What is the DAQ-STC?

The DAQ-STC is the system timing control application-specific integrated circuit (ASIC) designed by National Instruments and is the backbone of the 611*X* device. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into the following three groups:

- Analog input—two 24-bit, two 16-bit counters
- Analog output—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate are possible.

What does sampling rate mean to me?

It means that this is the fastest you can acquire data on your device and still achieve accurate results. The 611*X* device has a sampling rate of 5 MS/s. This sampling rate is at 5 MS/s regardless if 1 or 4 channels are acquiring data.

What type of 5 V protection does the 611*X* device have?

The 611*X* device has 5 V lines equipped with a self-resetting 1 A fuse.

Installation and Configuration

How do you set the base address for the 611*X* device?

The base address of the 611*X* device is assigned automatically through the PCI bus protocol. This assignment is completely transparent to you.

What jumpers should I be aware of when configuring my 611*X* device?

The 611*X* device is jumperless and switchless.

Which National Instruments document should I read first to get started using DAQ software?

Your NI-DAQ or application software release notes documentation is always the best starting place.

Analog Input and Output

I have connected a differential input signal, but my readings are random and drift rapidly. What's wrong?

Check your ground reference connections. Your signal may be referenced to a level that is considered *floating* with reference to the device ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the device reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of your output signal.

Can I synchronize a one-channel analog input data acquisition with a one-channel analog output waveform generation on my 611*X* device?

Yes. One way to accomplish this is to use the waveform generation timing pulses to control the analog input data acquisition. To do this, follow steps

1 through 4 below, in addition to the usual steps for data acquisition and waveform generation configuration.

1. Enable the PFI5 line for output, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.
2. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:
   - If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW).`
   - If you are using LabVIEW, invoke AI Clock Config VI with clock source code set to PFI pin, high to low, and clock source string set to 5.
3. Initiate analog input data acquisition, which will start only when the analog output waveform generation starts.
4. Initiate analog output waveform generation.

Timing and Digital I/O

What types of triggering can be hardware-implemented on my 611*X* device?

Hardware digital and analog triggering are both supported on the 611*X* device.

What added functionality does the DAQ-STC make possible in contrast to the Am9513?

The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. In fact, the DAQ-STC has the complexity of more than 24 chips. The DAQ-STC makes possible PFI lines, analog triggering, selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?

The DAQ-STC-based MIO devices have a 20 MHz timebase. The Am9513-based MIO devices have a 1 MHz or 5 MHz timebase.

Will the counter/timer applications that I wrote previously, work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs will still run. However, there are many differences in the counters between the 611*X* and other devices; the counter numbers are different, timebase selections are different, and the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on devices without the DAQ-STC).

If you are using the NI-DAQ language interface or LabWindows/CVI, the answer is no, the counter/timer applications that you wrote previously will not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions will not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

I'm using one of the general-purpose counter/timers on my 611*X* device, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using the NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are tri-stated.

What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using the NI-DAQ language interface or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, CTR Mode Config, and CTR Pulse Config advanced level VIs to indicate which

function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

Caution If you enable a PFI line for output, do not connect any external signal source to it; if you do, you can damage the device, the computer, and the connected equipment.

What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This means that the device circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Table 4-2, *I/O Signal Summary for the 611X*. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) will be in the high impedance state after power on, and Table 4-2 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor will set the DIO(0) pin to a logic high when the output is in a high impedance state.

D

Technical Support Resources

Web Support

National Instruments Web support is your first stop for help in solving installation, configuration, and application problems and questions. Online problem-solving and diagnostic resources include frequently asked questions, knowledge bases, product-specific troubleshooting wizards, manuals, drivers, software updates, and more. Web support is available through the Technical Support section of `ni.com`

NI Developer Zone

The NI Developer Zone at `ni.com/zone` is the essential resource for building measurement and automation systems. At the NI Developer Zone, you can easily access the latest example programs, system configurators, tutorials, technical news, as well as a community of developers ready to share their own techniques.

Customer Education

National Instruments provides a number of alternatives to satisfy your training needs, from self-paced tutorials, videos, and interactive CDs to instructor-led hands-on courses at locations around the world. Visit the Customer Education section of `ni.com` for online course schedules, syllabi, training centers, and class registration.

System Integration

If you have time constraints, limited in-house technical resources, or other dilemmas, you may prefer to employ consulting or system integration services. You can rely on the expertise available through our worldwide network of Alliance Program members. To find out more about our Alliance system integration solutions, visit the System Integration section of `ni.com`

Worldwide Support

National Instruments has offices located around the world to help address your support needs. You can access our branch office Web sites from the Worldwide Offices section of `ni.com`. Branch office Web sites provide up-to-date contact information, support phone numbers, e-mail addresses, and current events.

If you have searched the technical support resources on our Web site and still cannot find the answers you need, contact your local office or National Instruments corporate. Phone numbers for our worldwide offices are listed at the front of this manual.

Glossary

Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Symbols/Numbers

°	degrees
>	greater than
≥	greater than or equal to
<	less than
≤	less than or equal to
/	per
%	percent
±	plus or minus
+	positive of, or plus
–	negative of, or minus
Ω	ohms

$\sqrt{\ }$	square root of
+5 V	+5 VDC source signal

A

A	amperes
AC	alternating current
ACH	analog input channel signal
ACH0GND	analog input channel ground signal
A/D	analog-to-digital
ADC	analog-to-digital converter—an electronic device, often an integrated circuit, that converts an analog voltage to a digital number
AI	analog input
AIGATE	analog input gate signal
AIGND	analog input ground signal
ANSI	American National Standards Institute
AO	analog output
AOGND	analog output ground signal
ASIC	Application-Specific Integrated Circuit—a proprietary semiconductor component designed and manufactured to perform a set of specific functions.

B

bipolar	a signal range that includes both positive and negative values (for example, –5 V to +5 V)

C

C	Celsius
CalDAC	calibration DAC
CH	channel—pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels
cm	centimeter
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio—a measure of an instrument's ability to reject interference from a common-mode signal, usually expressed in decibels (dB)
CONVERT*	convert signal
counter/timer	a circuit that counts external pulses or clock pulses (timing)
CTR	counter

D

D/A	digital-to-analog
DAC	digital-to-analog converter—an electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition—a system that uses the computer to collect, receive, and generate electrical signals

DAQ-STC	Data acquisition system timing controller. An application-specific integrated circuit (ASIC) for the system timing requirements of a general A/D and D/A system.
dB	decibel—the unit for expressing a logarithmic measure of the ratio of two signal levels: dB=20log10 V1/V2, for signals in volts
DC	direct current
DGND	digital ground signal
DI	digital input
DIFF	differential mode
DIO	digital input/output
DIP	dual inline package
dithering	the addition of Gaussian noise to an analog input signal
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DNL	differential nonlinearity—a measure in least significant bit of the worst-case deviation of code widths from their ideal value of 1 LSB
DO	digital output

E

EEPROM	electrically erasable programmable read-only memory—ROM that can be erased with an electrical signal and reprogrammed
EXTSTROBE	external strobe signal

F

FIFO	first-in first-out memory buffer—FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be read or written. For example, an analog input FIFO stores the results of A/D conversions until the data can be read into system memory. Programming the DMA controller and servicing interrupts can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored in the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.
FREQ_OUT	frequency output signal
ft	feet

G

GATE	gate signal
GPCTR	general-purpose counter signal
GPCTR0_GATE	general-purpose counter 0 gate signal
GPCTR0_OUT	general-purpose counter 0 output signal
GPCTR0_SOURCE	general-purpose counter 0 clock source signal
GPCTR0_UP_DOWN	general-purpose counter 0 up down signal
GPCTR1_GATE	general-purpose counter 1 gate signal
GPCTR1_OUT	general-purpose counter 1 output signal
GPCTR1_SOURCE	general-purpose counter 1 clock source signal
GPCTR1_UP_DOWN	general-purpose counter 1 up down signal

H

h	hour
hex	hexadecimal
Hz	hertz

I

INL	integral nonlinearity–For an ADC, deviation of codes of the actual transfer function from a straight line.
I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
I_{OH}	current, output high
I_{OL}	current, output low

K

kHz	kilohertz

L

LED	light emitting diode
LSB	least significant bit

M

m	meter
MB	megabytes of memory
MHz	megahertz
MIO	multifunction I/O

MITE	MXI Interface to Everything
MSB	most significant bit
mux	multiplexer—a switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel
mV	millivolts

N

NC	normally closed, or not connected
NI-DAQ	National Instruments driver software for DAQ hardware
noise	an undesirable electrical signal—Noise comes from external sources such as the AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, electrical storms, welders, radio transmitters, and internal sources such as semiconductors, resistors, and capacitors. Noise corrupts signals you are trying to send or receive.
NRSE	nonreferenced single-ended mode—all measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground

O

OUT	output pin—a counter output pin where the counter can generate various TTL pulse waveforms

P

PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and work-stations; it offers a theoretical maximum transfer rate of 132 MB/s.

PFI	Programmable Function Input
PFI0/TRIG1	PFI0/trigger 1
PFI1/TRIG2	PFI1/trigger 2
PFI2/CONVERT*	PFI2/convert
PFI3/GPCTR1_SOURCE	PFI3/general purpose counter 1 source
PFI4/GPCTR1_GATE	PFI4/general-purpose counter 1 gate
PFI5/UPDATE*	PFI5/update
PFI6/WFTRIG	PFI6/waveform trigger
PFI7/STARTSCAN	PFI7/start of scan
PFI8/GPCTR0_SOURCE	PFI8/general-purpose counter 0 source
PFI9/GPCTR0_GATE	PFI9/general-purpose counter 0 gate
PGIA	Programmable Gain Instrumentation Amplifier
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output
ppm	parts per million
pu	pull-up

R

RAM	random access memory
rms	root mean square
RSE	referenced single-ended mode—all measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system
RTD	resistive temperature detector—a metallic probe that measures temperature based upon its coefficient of resistivity

RTSIbus	real-time system integration bus—the National Instruments timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise timing synchronization between multiple devices
RTSI_OSC	RTSI Oscillator—RTSI bus master clock

S

s	seconds
S	samples
SCANCLK	scan clock signal
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ devices in the noisy computer environment
SE	single-ended—a term used to describe an analog input that is measured with respect to a common ground
settling time	the amount of time required for a voltage to reach its final value within specified limits
signal conditioning	the manipulation of signals to prepare them for digitizing
SISOURCE	SI counter clock signal
SOURCE	source signal
S/s	samples per second—used to express the rate at which a DAQ device samples an analog signal
STARTSCAN	start scan signal
system noise	a measure of the amount of noise seen by an analog circuit or an ADC when the analog inputs are grounded

T

TC	terminal count—the ending value of a counter
t_{gh}	gate hold time
t_{gsu}	gate setup time
t_{gw}	gate pulse width
t_{out}	output delay time
THD	total harmonic distortion—the ratio of the total rms signal due to harmonic distortion to the overall rms signal, in decibel or a percentage
thermocouple	a temperature sensor created by joining two dissimilar metals. The junction produces a small voltage as a function of the temperature.
TRIG	trigger signal
t_{sc}	source clock period
t_{sp}	source pulse width
TTL	transistor-transistor logic

U

UI	update interval
UISOURCE	update interval counter clock signal
unipolar	a signal range that is always positive (for example, 0 to +10 V)
UPDATE	update signal

V

V	volts
VDC	volts direct current

VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program
V_{IH}	volts, input high
V_{IL}	volts, input low
V_{in}	volts in
V_m	measured voltage
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage
V_{rms}	volts, root mean square

W

WFTRIG	waveform generation trigger signal

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