Dynamics of neural motifs realized with a minimal memristive neurosynaptic unit

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Spiking neural networks (SNNs) require both neurons and synapses. Here we introduce a synaptic unit with both excitatory and inhibitory biomimetic dynamics (Rall's function). Combined with our previously introduced memristive spiking neuron, they complete a minimal model platform to build general SNNs. Our hardware neurosynaptic (NS) unit is fully analogue and implements a textbook theoretical model. It avoids the mismatch problem and is easily tunable at biocompatible timescales. We demonstrate the modularity of our NS-unit platform by building various basic neurocomputing primitives produced by basic motifs and their combination. With our novel hybrid theoretical and experimental approach we make three notable contributions: (1) We demonstrate that recursive inhibition (adaptation) and excitation can both be formulated as self-consistent dynamical problems. (2) We demonstrate that a minimal dynamical memory can be implemented with just one recursive single neuron. (3) We show that adopting a biomimetic membrane current in adaptive neuron models reveals an unknown connection to a cornerstone of physics, the harmonic oscillator model. Our NS unit realizes a building block for midsize SNNs of arbitrary geometry. Its simple design, along with the wide accessibility of ordinary electronic components, make our methodology an attractive platform to build neural interfaces for biological neuroscience, medical devices including deep brain stimulation, robotics, and artificial intelligence systems such as reservoir computing. We provide a bill of materials and printed-circuit-board designs to implement the device.

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I. INTRODUCTION: NEUROCOMPUTING PARADIGMS AND THE PROBLEM OF COMPUTING WITH SPIKES

Neuromorphic computing (NC) is a field aimed at implementing systems that can perform functions taking inspiration from the nervous system and brain. Examples range from face recognition through autonomous navigation to robotic motion, and many more that are revolutionizing modern life. To implement those systems, there are two main approaches. One is based on software running on digital computers, and the other is fabricating neuromorphic hardware that mimics the components of a neural network. In both cases, NC systems rely on models from theoretical neuroscience, computer science, or physics. Every model has a definition of its components, called neurons and synapses. Neurons are the degrees of freedom of a neural network, since they can be in different states. Synapses describe the couplings and interactions between them (see Fig. 1).

We recall a paradigmatic example of an NC system, the Hopfield model, to clarify the roles of neurons and synapses, which are often a matter of confusion. This is a model for associative memory, introduced in the 1980s [1]. It bears close similarity with magnetic spin models in physics (see Fig. 1). The neurons are defined as discrete variables, where $S_i = \pm 1$ denotes the ith member of the network. The synapses are the interactions between neurons, where the real parameter J_{ij} denotes the interaction between neurons i and j. The model has an energy given by the expression $E = (1/N)\sum J_{ij} S_i S_j$, where N is the number of neurons. Each memory corresponds to a local minimum of the energy landscape. The genius of Hopfield was to formulate a simple recipe to choose the J_{ij} couplings that provide such a landscape. The model can recall a memory by association. Namely, given an arbitrary initial state S_i for $i = 1, \ldots, N$, an algorithm of energy minimization will retrieve its associated memory.

A. Neurocomputing with software

The Hopfield model, as any of the modern deep neural networks for artificial intelligence, is an algorithm implemented in software that runs on digital computers. The computers may be conventional or the so-called "neuromorphic chips," such as TrueNorth or Loihi, which are digital processors with an optimized architecture to run those types of models [2]. Bitlike variables and J_{ij} couplings are the simplest modeling for neurons and synapses and allow for computation with massive neural networks, such as those used in artificial intelligence. However,

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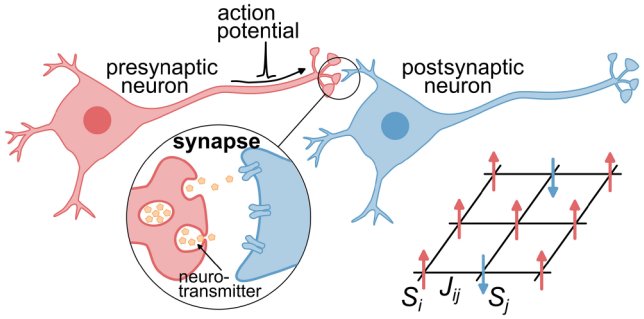

FIG. 1. Schematic view of the presynaptic (red) and postsynaptic (blue) neurons. The neurons are coupled by a synapse. The action potential reaching the end of the axon terminals of the preneuron induces a synaptic input current in the postneuron, which can be excitatory (positive) or inhibitory (negative). The inset shows the analogy with the Hopfield model, where neurons are spins S_i, and synapses are the couplings J_{ij} .

severe limitations emerge quickly if one wants to adopt a more biomimetic spiking-neural-network (SNN) model.

In fact, neurons and synapses are qualitatively different than the simplified description of the Hopfield model: they are *dynamical systems*. Neurons are a special type of cell in the body that are characterized by having electrical activity. They are not just active or inactive, but emit action potentials that are fast voltage spikes. Synapses involve the dynamical process of transferring neurotransmitters between a presynaptic and a postsynaptic neuron, so they are not just real-valued parameters (see Fig. 1) [3].

The dynamical models of spiking neurons range from schematic to biorealistic. In the first case, the most paradigmatic one is the leaky-integrate-and-fire (LIF) model [3,4]. For the latter, the most famous one is the Hodgkin-Huxley model, which describes the generation of action potential in the giant axon of the squid [5]. These models are described by multiple nonlinear differential equations. Similarly, to describe the synaptic couplings, further differential equations are needed. Hence, to numerically study an SNN requires the solution of a challenging system of multiple coupled nonlinear differential equations. The scaling of these SNNs is typically bad, as the number of differential equations grows rapidly with the size of the network and its synaptic connectivity. Possibly an even more serious problem is the scaling of the simulation time. An action-potential spike typically lasts 1 ms, and the firing rate of a neuron is roughly between 1 and 100 Hz. Thus a time step of 0.1 ms is often adopted. The timescale associated with the global behavior can be considered of the order of minutes, so there is at least a 10^6 factor for the number of simulation time steps, just for one neuron. However, this scaling quickly worsens with a growing number of neurons, at least by a factor of N, in the most favorable case. Nevertheless, there are several implementations of useful numerical simulators of SNNs available (see [6] for a recent review and benchmark).

It is not easy to find out what is the largest SNN size that current simulators can handle [6], as this depends on the model, the connectivity, the computer architecture, the power, etc. Whatever this estimate may be, it would become severely reduced if one considers continuous models, without hard resets of variables, where the spike emission is not described by time stamps and synapses are dynamical. Namely, where the full nonlinearity of the problem is properly treated.

Finally, another severe limitation imposed on software approaches is the numerical and electric power requirements needed to carry out the computation. Power efficiency becomes a relevant aspect, especially for practical applications such as navigation control, neuroprostheses, wearable implants, brain-machine interfaces, etc. [7,8].

B. Neurocomputing in hardware

A very different approach to NC is based on the idea of implementing neurons and synapses directly in hardware. In fact, a hardware implementation has the very attractive feature of *ideal scaling* because time represents itself. In other words, the system evolves in real time and the time evolution occurs irrespective of the number of neurons in the network. If it takes one minute to simulate the behavior of one neuron, it takes the same one minute to simulate the behavior of a network of size N.

Modern silicon electronic technology based on complementary metal oxide semiconductor (CMOS) systems can implement, *a priori*, almost any desired mathematical model. This approach has had several decades of development, starting with the pioneering work of Mead, who coined the term "neuromorphic electronics" [9]. He observed that transistors operating in the subthreshold regime, i.e., not as digital switches but as variable conductances, show a behavior analogous to the activation of ionic channels in neuron membrane models. There are currently many electronic chips that integrate millions of *silicon neurons*, which typically require tens of transistors each [10,11]. Surprisingly, the implementation of dynamical synapses in hardware has received comparatively less attention [12], although they are a key feature in theoretical neuroscience [13].

A remarkable example of this type of hardware implementation is the DYNAP-SE chip, which counts 4×256 neurosynaptic computing units [14]. Each one implements an adaptive-exponential integrate-and-fire neuron [3] that generates discrete spike events, plus a dynamical synapse that can implement biomimetic currents. This chip exhibits the appealing feature of ultralow power consumption. In contrast, some significant inconveniences of this approach are that it requires a high level of technical expertise and of fabrication capabilities, beyond the reach of most

research labs, and that it lacks flexibility, as it takes years to design and implement each electronic chip. Nevertheless, the most significant of all issues, common to all other electronic implementations that work in the transistor subthreshold regime, is that it suffers from a severe problem of device mismatch [15].

Here we propose to take a drastically alternative approach to fabricating, studying, and understanding SNNs. While current CMOS VLSI may be considered as a *top-down* method, where fabricating a large number of units is a main goal, here, we propose a *bottom-up* approach. Our methodology is constructive, with neurosynaptic units that can be modularly interconnected to implement neurocomputing primitives. Crucially, we can do this in a fully controlled manner, including the homogeneity between the spiking units, hence mitigating the mismatch problem. Thus, our approach to implementing SNNs in hardware qualitatively differs from all others in multiple aspects: it is of extreme simplicity, extreme flexibility, extreme tunability, controlled reproducibility, very low fabrication cost, and based on theoretical neuroscience textbook modeling.

Here, we shall introduce and demonstrate our hybrid theoretical and experimental methodology by implementing in hardware all the basic neurocomputing motifs from theoretical neuroscience. The originality and value of our approach will be highlighted by the relevant novel results and insights that emerge from the study of dynamical systems.

Specifically, here we shall demonstrate the following important results.

(1) We demonstrate that the minimal recursive SNN, i.e., a single neuron with either autoinhibition (adaptation) or autoexcitation, can be mapped onto a self-consistent dynamical problem with a geometrical representation. Based on this formulation and its hardware implementation we demonstrate the two following important results.

(2) For the case of autoexcitation, we obtained the unprecedented realization of a single-neuron stable dynamical memory (also known as a working memory). This is significant, because in the current literature it is widely assumed that, to achieve a stable working memory, a recursive neuron assembly is needed [3]. This finding may also explain the recent striking experimental observation of the bump of activity in the head direction system of *Drosophila*. This is realized in a neural structure called the ellipsoidal body, which counts with only a handful of neurons [16].

(3) For the case of autoinhibition, we made two significant findings. First, we show that our model is a hardware counterpart of paradigmatic models of theoretical neuroscience, the Izhikevich and the AdEx [3,17]. Similarly to those models, the adaptation is mediated by a spike-dependent membrane current. But, improving on them, we model the current with the more biorealistic Rall's function [13]. This yields the second significant finding, where we theoretically show that the model can be mapped to a cornerstone model of physics, namely, the driven harmonic oscillator with friction. We also demonstrate this experimentally, by the measured currents in our hardware circuits that realize an intrinsic burster or pacemaker state.

(4) We show how the single-neuron motifs can be leveraged as components of higher-level two-neuron motifs, which produce three different types of central pattern generators (CPG). Our results demonstrate two features: (i) the modular constructive nature of our methodology; and (ii) that our CPGs can easily work at biocompatible timescales, making them ready for deployment in practical applications.

The paper is organized as follows. In Sec. II we first describe the neurosynaptic unit model and its circuit implementation, emphasizing the connection to mathematical models and its full parameter tunability. Then, in Secs. III and IV we demonstrate the implementation of the simplest motifs of spiking neural networks, that realize *neuromorphic primitives*, i.e., basic neurocomputing functions. Then, in Sec. V we discuss how our present work is related to the intense activity in the search for memristive materials. We also make some general remarks about the positioning of our approach with respect to other hardware in regard to power efficiency. In the final Sec. VI we conclude with a recap on the main contributions of our present work both for science and in neuromorphic electronics. Finally, in the Appendix we provide technical details on all our circuits and a list of materials, which are also available upon reasonable request.

II. NEUROSYNAPTIC UNIT: THEORETICAL MODEL AND ITS PHYSICAL EMBODIMENT

A. Theoretical model

The neurosynaptic (NS) hardware unit takes inspiration from a basic model in Wilson's textbook on theoretical neuroscience (cf. Ch. 12 of Ref. [13]). It is a set of differential equations for a spiking neuron of type I supplemented with synaptic currents. A type-I neuron, such as a cortical neuron [13,18], characteristically fires action potential spikes at arbitrarily low rates.

When a presynaptic (or upstream) neuron emits a spike, which is a very fast event, typically lasting 1 ms, the action potential liberates a certain amount of neurotransmitters (see Fig. 1) into the synaptic cleft, which is about 20 nm wide [19]. Those molecules reach the dendrites of the postsynaptic (or downstream) neuron where they open ionic channels that induce synaptic currents integrated in the cell body. The neurotransmitters can be either excitatory or inhibitory, depending on whether they contribute or prevent the emission of a spike by the postsynaptic neuron. This depends on the sign of the synaptic current: if positive, or depolarizing, it brings the potential of

the neuron closer to the firing threshold; if negative, or hyperpolarizing, it has the opposite effect.

This synaptic current process typically occurs in the range of tens to hundreds of milliseconds, thus at a much longer timescale than the spike emission, and has its own dynamics. This introduces an additional and relevant timescale in SNN dynamics, which is well recognized to have significant consequences [20].

In the 1960s Rall introduced a set of differential equations to model this phenomenon, which has been widely adopted [3,13,21,22]. When applied to a delta function representing the sharp spike emission, they provide as a solution a synaptic current with the functional form known as Rall's alpha function, $\alpha(t) = (t/\tau_s^2)\exp(-t/\tau_s)$. Thus, the sharp ($\sim 1$ ms) spike emitted by the preneuron is perceived by the postneuron as a broad synaptic current input that peaks and decays in a typical timescale τ_s ($\sim$ 10–100 ms).

Rall's differential equations for the synaptic current are incorporated in Wilson's book model (cf. Eq. (12.18) of Ref. [13]). Those equations, along with the expression for a general integrate-and-fire spiking neuron from Gerstner's book (cf. Eq. (5.2) of Ref. [3]), conform to the mathematical model that underlies our hardware implementation. The set of equations reads

$$C_m \frac{dV_m}{dt} = f(V_m) + I_\alpha + I_0, \tag{1}$$

$$\tau_s \frac{dI_e}{dt} = -I_e + I_\delta H(V_{\text{pre}} - \Omega), \tag{2}$$

$$\tau_s \frac{dI_\alpha}{dt} = -I_\alpha + I_e. \tag{3}$$

Here V_m is the neuron's membrane potential; C_m is the membrane capacitance; $\tau_s = R_s C_s$ is the synapse time constant, with C_s and R_s being the capacitance and leak resistance of the synapse, respectively; I_0 is an external input current to the neuron; and I_e and I_α are dynamical synaptic currents (analogous to f and g in Wilson's book [13]). Also closely following the notation of Wilson, H denotes a step function (or Heaviside function) that is unity if the presynaptic voltage V_{pre} is larger than the synaptic threshold Ω, or zero otherwise [13]. Thus, the presynaptic action potential is modeled as a narrow pulse of rectangular shape that represents a $\delta(t)$-like spike. The condition $(V_{\text{pre}} > \Omega)$ sets the width of the narrow pulse, which we call τ_a, and its magnitude we denote by I_δ. Hence, this spike carries a charge

$$Q_N = I_\delta \tau_a \tag{4}$$

that physically may represent the amount of neurotransmitter liberated by the preneuron into the synapse.

The current I_e results from the first leaky integration equation (2) of the sharp rectangular current pulse. Hence, with $\tau_a \ll \tau_s$, one obtains the exponential current

$$I_e(t) = \frac{Q_N}{\tau_s} \exp(-t/\tau_s), \tag{5}$$

This current is the input to the third equation (3), so after this second leaky integration one gets the alpha function [3,13,22]

$$I_\alpha(t) = \frac{Q_N}{\tau_s} \frac{t}{\tau_s} \exp(-t/\tau_s). \tag{6}$$

These currents have biomimetic line shapes [3,13]. They realize the synaptic currents of four basic types, namely, fast exponential excitatory (AMPA) or inhibitory ($GABA_a$), and slow alpha-function excitatory (NMDA) or inhibitory ($GABA_b$) (cf. Ch. 3 of Ref. [3]).

B. Analog leaky-integrate-and-fire model

To fully specify the model, we need to define the nonlinear function $f(V_m)$ in Eq. (1) that generates the spikes. In the interest of simplicity, we start by recalling the leaky-integrate-and-fire (LIF) model, which is the most widely used. In the LIF model, shown in Fig. 2, the body (soma) of the neuron is represented as a capacitor C_m that charges by integrating the input ionic currents arriving at its dendrites. This integration suffers leakage losses, which are represented by the membrane resistor R_m. The third component of the LIF model is a voltage-dependent switch S that is normally open, but closes when the potential $V_m(t)$ on the capacitor reaches a threshold V_{th}. At that point, one says that a spike is "fired" at a time $t = t_{\text{fire}}$, the voltage V_m is reset to a low resting value, and the switch is set back to open. It is important to realize that the LIF model is a mathematical model and the spike is an abstract "event" defined by the condition $V_m = V_{\text{th}}$ [3]. In other words, there is no dynamical description of the spike [23]. In this model, the nonlinear function $f(V_m)$ is implemented by the V-dependent switch.

Here, we shall adopt the above idealized description as a basis for our hardware implementation, which we shall also augment to provide an embodiment of the physical emission of an action-potential spike (see Fig. 2). The first step is, as shown in Fig. 2, to add a small "load" resistor with $R_a \ll R_m$. Then, when S closes at $V_m = V_{\text{th}}$, the C_m quickly discharges on R_a and the current on this resistor produces a voltage spike. The fast discharge time is $\tau_a = R_a C_m$, which provides a definite parametrization to the width of the δ-like spike that we mentioned above Eq. (4). Interestingly, we may give this spike generation mechanism a biological interpretation as the action potential that is initiated in the axon hillock [24]. The axon hillock is characterized by a high concentration of Na channels, over 100 times more than in the cell body (soma) [25]. We can thus think of the closing of the V-dependent

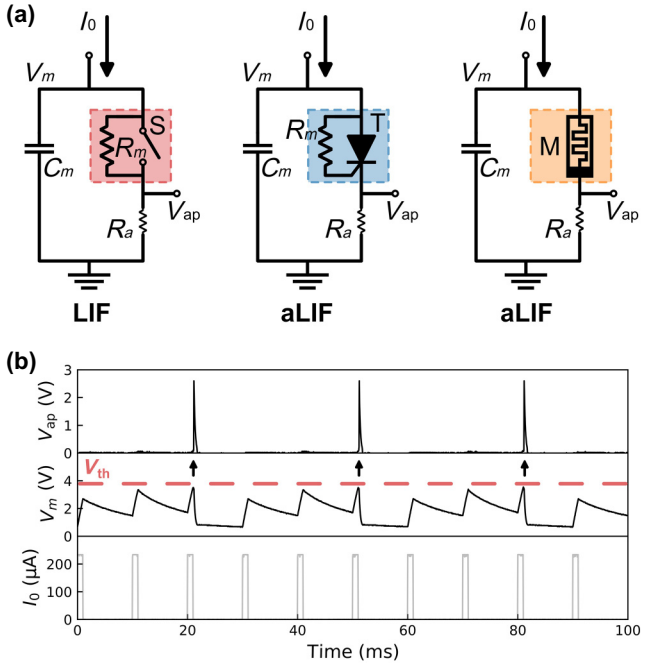

FIG. 2. The analog-LIF model: (a) The leaky-integrate-and-fire model with a voltage-dependent switch S is augmented with a discharge resistance R_a to produce an explicit action potential (left panel). The switch can be implemented by a thyristor T with a resistor R_m between its gate and anode. This resistor also provides the leak resistance of the model, while the thyristor is not conducting (middle panel). The combination of $T + R_m$ realizes the concept of a memristor, with the functionality of a voltage-gated conductance, central to all neuron models (right panel). (b) LIF behavior: The input current pulses (bottom panel) are leaky integrated, producing the increase of the membrane voltage V_m (center panel). When V_m reaches the dynamical threshold $V_{\rm th}$ (vertical arrows), the forward resistance of the T collapses and there is the emission of an output of a continuous action-potential spike $V_{\rm ap}$ (top panel). Circuit technical details and parameter values for all figures are provided in the Appendix.

switch as representing the massive opening of those channels and the enhanced membrane conductance at the axon hillock described by the small resistance R_a. Despite the extended use of the LIF model, we are not aware of this simple extension.

The second step to specify the embodiment of the model is to implement the V-dependent switch. The simplest circuit to do this exploits the concept of a *volatile memristor*, which is a V-dependent resistance (or V-gated conductance) [26]. We have recently, demonstrated that a combination of a thyristor and a resistor can implement such a memristive two-terminal device that provides the desired functionality [27,28].

A voltage-gated conductance is in fact a key ingredient common to all conductance-based neuron models, such as Hodgkin-Huxley, Morris-Lecar, Hindmarsh-Rose, etc. [13]. Those theoretical models are formulated with differential equations that describe the spike emission as a *continuous* dynamical process. It results from the strong nonlinearity of the equations, namely the property of excitability [13]. We note that simplified models, such as Izhikevich and AdEx [3], which are popular for numerical simulations, do not fall in that category. This is because they require a discontinuous reset, for the sake of their numerical simplicity [3,23].

Our memristor spiking model implementation is shown in Fig. 2 and it is described by the following equations:

$$C_m \frac{dV_m}{dt} = -\frac{V_m}{R_m[S] + R_a} + I_0, \tag{7}$$

$$V_{\rm ap} = \frac{V_m}{R_m[S] + R_a} R_a. \tag{8}$$

Here $R_m[S]$, with high (hi) or low (lo) S, denotes a volatile memristor whose resistance can switch between two states: a high resistance R_m[hi] and low resistance R_m[lo]. The commutation depends on the applied voltage, thus $S = S(V_m)$, implementing a V-dependent conductance [28]. Equation (8) is a voltage divider providing the action potential $V_{\rm ap}$ on the axon-hillock resistor R_a. When the memristor is in the R_m[hi] $\gg R_a$ state (i.e., open switch), then $V_{\rm ap}$ is negligible. When it commutes to R_m[lo] $\ll R_a$ (i.e., closed switch), there is an action-potential spike explicitly described by $V_{\rm ap}(t)$ (see Fig. 2).

Notice that the first differential equation above may seem linear, but it is not. In fact, the nonlinearity, necessary for the excitability of the model, is provided by the commutation property of the memristor device [28].

The circuit implementation of the LIF model that we just described features a fully continuous spike generation mechanism. Therefore, our circuit model, although not bio-realistic but biomimetic, can be considered as a member of the class of *conductance-based* neuron models and we call it the analog-LIF (aLIF) model. In Fig. 2 we show the measured traces of the neuron circuit, which shows the leaky integration of input current pulses and the resulting output emitted spikes $V_{\rm ap}(t)$.

C. Physical embodiment of the neurosynaptic model equations

One of the main goals of the present work is to provide a simple and transparent physical instantiation of the set of equations (1)–(3), which are the mathematical reference. We would like that each circuit component could be directly related to the theoretical model parameters. Furthermore, we would like the hardware implementation to be modular, such that the subcircuit units can be associated to build arbitrarily spiking neural networks, and eventually a neurocomputer. We shall see in the rest of the paper that all these goals are accomplished by the NS unit that we describe below.

For the spiking generation mechanism, which is encoded in Eq. (7), we adopt the aLIF circuit model discussed in the previous section. Thus, we rewrite below the reference model equations (1)–(3) including the aLIF and renaming some variables for convenience:

$$C_m \frac{dV_m}{dt} = -\frac{V_m}{R_m[S] + R_a} + I_{s2} + I_0, \tag{9}$$

$$V_{\text{post}} = \frac{V_m}{R_m[S] + R_a} R_a, \tag{10}$$

$$\tau_s \frac{dI_{s1}}{dt} = -I_{s1} + I_\delta H(V_{\text{pre}} - \Omega), \tag{11}$$

$$\tau_s \frac{dI_{s2}}{dt} = -I_{s2} + I_{s1}. \tag{12}$$

Here $V_{\text{post}} = V_{\text{ap}}$ denotes the output postsynaptic action potential, and I_{s1} and I_{s2} denote the synaptic currents of the two leaky-integration stages.

Similar to what was provided for spike generation via the aLIF circuit, the synaptic current equations (11) and (12) also have a concrete physical embodiment, as we show in the circuit in Fig. 3. We indicate in the figure the correspondence between the equations of the model and the circuit blocks. We shall now describe the implementation in detail. For the sake of clarity, we shall explain the circuit in Fig. 3 from input to output, i.e., from the presynaptic neuron on the left (V_{pre}) to the postsynaptic neuron on the right (V_{post}).

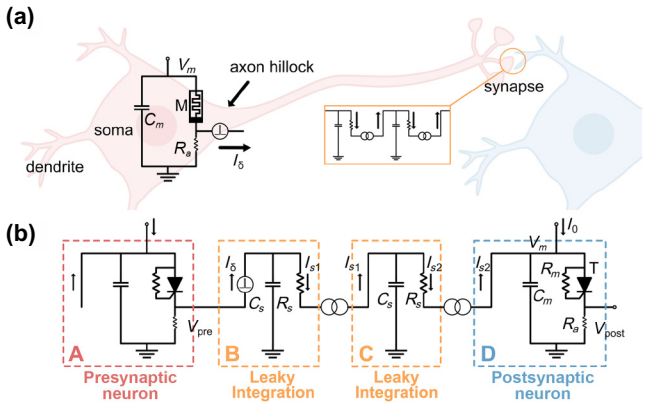

FIG. 3. (a) Schematic diagram of the neurosynaptic unit circuit blocks and their relation with the biological neuron. (b) Physical embodiment of model equations (9)–(12) with subcircuit blocks denoting the pre- and postsynaptic neurons and the synaptic block in between. The synaptic block has two stages that perform a leaky integration each. The input presynaptic potential produces a $\delta(t)$-like current spike. A double leaky integration of the pulse provides an $\alpha(t)$-like synaptic current into the postsynaptic neuron, which also receives the external input I_0.

1. Neurosynaptic circuit blocks

a. The first block. A is an aLIF representing the presynaptic neuron. It generates the action potential spike V_{pre} that is the input to the NS unit. It was described in detail before.

b. The second block. B implements the differential equation (11) of our model. The current term $I_{s1}(t)$ is the dynamical variable and $I_\delta H(V_{\text{pre}} - \Omega)$ is an independent term.

The $I_\delta(t)$ currents are rectangular pulses emitted by each spike V_{pre}. Their width is τ_a (see Sec. II B) and their intensity is controlled by a resistor R_W in a conventional current-source implementation. The technical details are provided in the Appendix. Here, it is important to mention that R_W controls the synaptic coupling that is denoted W_{ij} between neurons i and j, in the terminology of artificial neural networks.

These W_{ij} couplings are key parameters for networks that implement synaptic learning, such as through spike time-dependent plasticity [3]. In that case, one may adopt nonvolatile memristors for the R_W, as we shall discuss elsewhere.

The synaptic current pulse I_δ has a short duration, so it approximates a delta function I_δ that is leaky integrated by the R_sC_s pair. This circuit provides the time constant τ_s and implements the differential equation in the current $I_{s1}(t)$, which is the output of the second block.

c. The third block. C implements Eq. (12) in a similar fashion. There, the current $I_{s2}(t)$ is the dynamic variable and the current I_{s1} enters as the independent term. To do this we need to take I_{s1} output from the second block and input it to the third one. The tricky part is to "copy the current" from one to the other, independently of the load represented by the latter. We resolve this by a standard electronic circuit, aptly called a "current mirror" (CM), and provide the technical details in the Appendix.

We note a useful feature of our CM implementation, namely, given the input, the output can be chosen *either* positive or negative in polarity. This feature is extremely convenient, as we can implement either excitatory or inhibitory synaptic currents. In other words, this feature allows one to choose the sign of the synaptic coupling parameters W_{ij} in an artificial neural network.

This circuit block leaky integrates the input current I_{s1} with timescale constant $\tau_s = R_sC_s$, similarly as the previous stage. The output of this block is the current signal $I_{s2}(t)$ and the same CM solution is adopted to input it (or its negative copy) to the last block, which is the aLIF circuit of the postsynaptic neuron.

d. The last block. D implements Eqs. (9) and (10), i.e., the aLIF neuron model [28]. This subcircuit has already been discussed in detail above. Here we just note that it corresponds to the *postsynaptic* neuron, so the action-potential spike emitted by this last block is denoted by $V_{\text{post}}(t)$.

2. Synaptic current forms

The reader may have realized that our implementation provides the freedom to adopt either one or two leaky integration synaptic blocks. If only one (yellow in Fig. 3) block is used, the single spike input I_δ is transformed into $I_{s1}(t) \sim \pm\exp(-t/\tau_s)$. While, if two blocks are adopted, the resulting output to a single input I_δ spike is $I_{s2}(t) \sim \pm\alpha(t/\tau_s)$.

In Fig. 4, we show an example of the temporal traces of the currents at different points of the NS-unit circuit of Fig. 3. The first one is the presynaptic action-potential spike, the output of box A in Fig. 3, which shows the triangular shape produced by the fast discharge of C_m on R_a with $\tau_a \sim$ milliseconds, as we described before. This presynaptic potential, through the condition $V_{\text{pre}} > \Omega \approx 0.7$ V in our implementation (see the Appendix), produces the $I_\delta(t)$ current pulse, which is input to box B. It has duration $\sim \tau_a$ and intensity $I_\delta \approx V_+/R_W$, where V_+ (≈ 4 V) is set by the circuit voltage source (see the Appendix). The sharp pulse is then leaky integrated [cf. Eq. (11)] to produce the synaptic current $I_{s1}(t)$ with the exponential form as in Eq. (11), at the output of box B. The second leaky integration produces the synaptic current $I_{s2}(t)$ with the alpha form as in Eq. (12), at the output of box C. As shown by the good quality of the fits in Fig. 4, the NS faithfully implements those functional forms and keeps constant the normalization of the integrated charge Q_N to a reasonably good approximation.

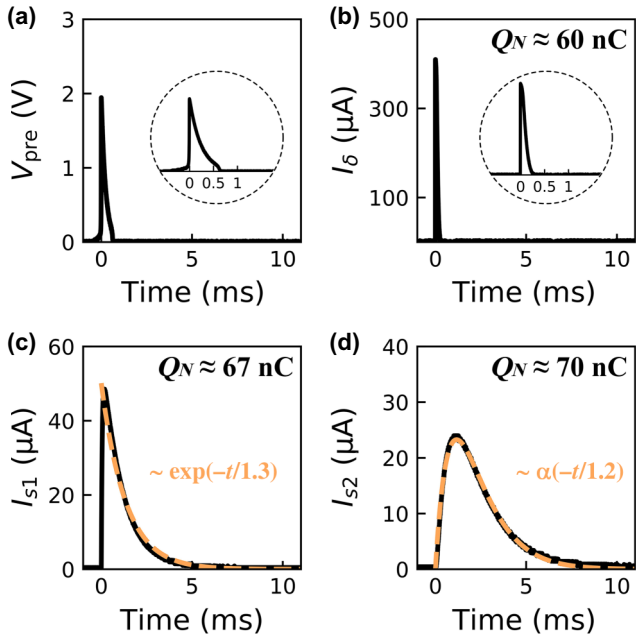

FIG. 4. Traces at the different stages of the NS unit. (a) The presynaptic neuron action-potential spike is the input to the NS unit. (b) The action potential is transformed into a $\delta(t)$-like pulse with an intensity I_δ (modulated by R_W) and a duration given by the spike emission time $\sim \tau_a$. The pulse carries a total "neurotransmitter" charge $Q_N \approx I_\delta \tau_a$. (c) First leaky-integration stage [Eq. (11)], which provides and exponential current I_e=I_{s1} with timescale $\tau_s = RsCs$, where Q_N is the time integral of the current. (d) Second leaky-integration stage [Eq. (12)], which provides an $\alpha(t)$-like synaptic current $I_\alpha = I_{s2}$. Note that, as in the mathematical model, both Q_N and τ_s remain constant (to a reasonable approximation) after each successive leaky integration. They are also in reasonably good agreement with the nominal parameter values $Q_N \approx 80$ nC [calculated from Eq. (15)] and $\tau_s = 1.6$ ms.

3. Synaptic current versus conductances

There is one important point about our implementation that is worth clarifying here. Theoretical models are formulated in terms of either membrane conductances or synaptic currents (see Ch. 3 and Fig. 3.2 in Ref. [3]). However, we shall show that these two options are essentially the same.

The key point is to realize that neurons spend most of their time at and around their resting potential, $V_m \approx V_{\text{rest}} \approx -70$ mV. The potential V_m slowly drifts up or down under the influence of synaptic currents. Eventually, a small upward change of about 10 mV drives the neuron to emit a short action-potential spike and quickly returns to $V_m \approx V_{\text{rest}}$. The general expression of synaptic currents in theoretical models reads [3]

$$I_{\text{syn}}(t) = -g_{\text{syn}}(t)(V_m(t) - E), \tag{13}$$

where $g_{\text{syn}}(t)$ is the synaptic conductance and E is a constant potential parameter, which is chosen either higher or lower than V_{rest} for excitatory or inhibitory currents, respectively [3,13]. Hence, from $V_m(t) \approx V_{\text{rest}}$ all the time except in brief firing events lasting a few milliseconds, to a good approximation, the temporal dependence of I_{syn} is the same as $g_{\text{syn}}(t)$, so one can model either. This feature is also the reason why one often reads in the neuroscience literature expressions such as "to inject a conductance" [29].

D. Synaptic current timescales: spike by spike to rate coding

An important question in neuroscience is what is the nature of the neural code. In neural networks, do neurons code through the timing between spikes or by the neuron spiking rate? Our neurosynaptic unit is well equipped to implement both of these representations. The key parameters to compare are the timescale for successive spike

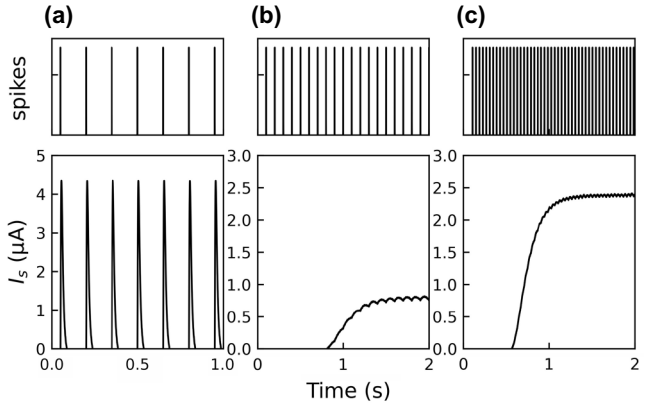

FIG. 5. (a) Spike-by-spike coding. Each emitted presynaptic spike (top) produces individual α-type spikes of synaptic current (bottom). (b),(c) Rate coding. The presynaptic emitted spikes (top) have a high rate and produce a synaptic current buildup by accumulation or leaky integration (bottom). The current intensity encodes the spiking frequency rate, $I_s = I_s(f)$.

emission, i.e., the membrane timescale $\tau_m \sim R_m C_m$, versus the synaptic integration timescale $\tau_s \sim R_s C_s$.

If $\tau_s \leq \tau_m$ then the synaptic leaky integration can follow individual spike emission and spike-by-spike time coding is possible. On the other hand, if $\tau_s \geq \tau_m$, the effect of the successive spikes gets accumulated and a synaptic current I_s proportional to the firing rate f results. In Fig. 5 we illustrate the different coding regimes. We show the input spikes V_{pre} of a presynaptic neuron acting on the synaptic unit (cf. Fig. 3) and the resulting output synaptic currents I_{s2} that it generates.

To determine whether the system is in the spike-by-spike or rate-coding regime, we need to consider the activation function of the neuron model $f(I_{\text{in}})$ that is shown in Fig. 6. The frequency or equivalently the interspike interval $\text{ISI} = 1/f$ depends on the external input current excitation, so it is more accurate to compare this timescale (instead of τ_m) with the leaky-integration timescale τ_s. Hence, per our previous discussion, we have that $1/f > \tau_s$ would correspond to spike-by-spike coding, while $1/f < \tau_s$ would correspond to the rate-coding mode. Thus, higher spiking frequencies naturally correspond to the rate-coding regime, and this is well illustrated in Fig. 5

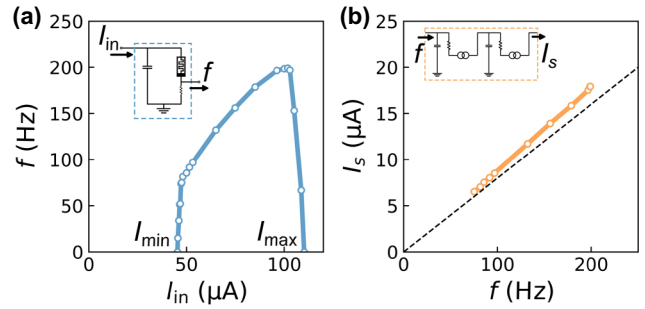

FIG. 6. Response functions of neuron and synapse subcircuit units. (a) The spiking rate as a function of the input current, $f(I_{\text{in}})$, produced by the aLIF neuron subcircuit (box D in Fig. 3). Here I_{min} denotes the threshold of excitation and I_{max} the value where the neuron stops spiking. (b) The synaptic current $I_s(f)$ of the leaky-integrator subcircuit (boxes B and C in Fig. 3) in the spike rate regime. The slope is given by the neurotransmitter charge Q_N, as in Eq. (14). The dashed line shows the theoretical $I_s(f)$ for the nominal value of Q_N computed with Eq. (15).

We may make here a side comment on the activation function $f(I_{\text{in}})$. As shown in the Fig. 6 this function also exhibits a maximal current threshold I_{max}, where the firing frequency suddenly decreases down to zero [28]. This is actually a biomimetic property of our neuron model. The eventual decrease of the spiking frequency at high current excitation is a phenomenon that is observed in biological neurons, where is known as "depolarization block" [30]. It is often considered relevant for the understanding of epileptic seizures [31].

It is an important question to determine what controls the intensity of the synaptic current in the rate-coding mode. We have discussed in Sec. II C 2 how the intensity of the synaptic current that is produced by a single action-potential spike is controlled by the resistor R_W. More specifically, we showed that for spike-by-spike coding, R_W controls the total charge due to a single spike, i.e., $Q_N = \int I_s\, dt$. This charge per spike is *conserved* across the leaky-integration stages, i.e., there is no current amplification.

For the rate-coding case, the successive spikes are accumulated, hence we expect that the synaptic current will be given by $Q_N f$. A subtle point to note, however, and as seen in Fig. 5, is that the accumulation takes a certain time to reach a steady state, which is the leaky-integration time constant τ_s. Therefore, after the transient integration time, we have

$$I_{se} \approx Q_N f \tag{14}$$

for the excitatory case. This simple relation is in good agreement with our circuit measurements shown in Fig. 6, including the quantitative value of the slope $Q_N \approx 80$ nC (see Fig. 4).

We may provide the explicit dependence of Q_N with the circuit model parameters. Recalling the expression for the charge contribution of each spike, we have

$$Q_N \approx I_\delta \tau_a \approx (V_+/R_W) R_a C_m. \tag{15}$$

Finally, we should note that all the previous considerations also remain valid for the case of inhibitory synaptic currents (since we just change the polarity of the last current mirror). Hence, in that case the $I_s(f)$ response function is simply the reflection of Eq. (14), namely,

$$I_{si} \approx -Q_N f. \tag{16}$$

III. RESULTS

A. Basic spiking-neural-network motifs and neurocomputational primitives

The methodology that we described above, in terms of circuit blocks, is modular, and therefore is well adapted to implement arbitrary biomimetic SNNs. In the next sections, we shall illustrate how one can establish basic network motifs, such as a single neuron with synaptic self-excitation or self-inhibition, and then two mutually inhibiting neurons. The spiking states of these motifs realize neurocomputational functions or primitives.

The basic motifs that we shall consider are shown in Fig. 7. The simplest motif is, of course, an isolated spiking neuron. We have already discussed its behavior in Sec. II B. The first nontrivial motifs display self-feedback, which is the simplest case of a recursive SNN. The self-excitatory case provides an instantiation of an important neurocomputing primitive, called dynamical memory, short-term memory, or simply activity "bump." The second case is a self-inhibitory neuron, which implements two other important neural primitives: spiking adaptation and bursting [3,13].

Then, we shall leverage those basic primitives to build more complex two-neuron SNNs. We shall consider two different motifs, and implement three different types of central pattern generators (CPGs) [13,32]. These are also fundamental neuronal functions that are widely studied, as they broadly appear in neuroscience [33,34] and robotics

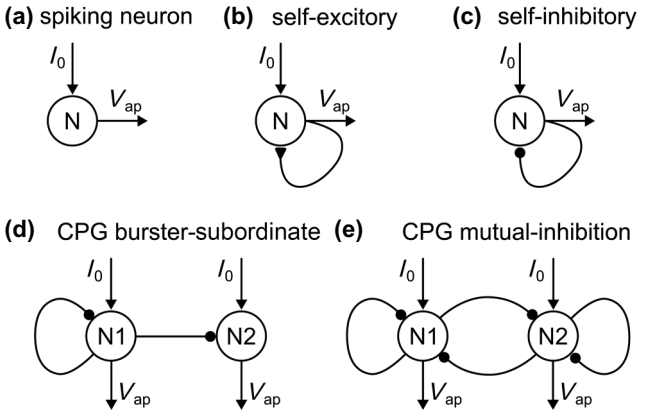

FIG. 7. SNN motifs. (a) Single spiking neuron. (b) Single spiking neuron with excitatory feedback. This motif represents both an autapse (self-axon-dendrite connection) or an intrinsic excitation current, like the inward Ca^{2+}, I_T. (c) Single spiking neuron with inhibitory feedback. This motif represents both an autapse or an intrinsic adaptation current, like the hyperpolarizing I_{AHP} that is also mediated by Ca^{2+} (see Sec. 10.3 of Ref. [13]). (d) CPG primary-subordinate motif with a burster neuron (primary) that inhibits a regular spiking neuron (subordinate). (e) CPG of mutually inhibiting neurons with self-adaptation. The same motif has two cases: two bursters or two frequency-adaptation neurons, which give qualitative different traces.

[35,36]. While in the present introductory work, we shall stop at two-neuron motifs, it should be clear that the present methodology is general and permits building larger SNNs with arbitrary architecture.

B. Self-excitation: Activity bump and dynamical memory

In this section, we begin with the simplest motif: a self-excitatory neuron (see Fig. 7). This simple motif brings a significant surprise: contrary to the common wisdom, it is sufficient to implement a basic neurocomputational primitive, namely, a dynamical memory [3]. Indeed, it is expected for a single neuron with a self-excitatory feedback to show a runaway rate, and that a population of neurons is needed to achieve a stable self-excitation [3]. Here, we shall demonstrate that this is not the case by explicitly exhibiting the dynamical memory in hardware and also its stability against strong perturbations.

The reverberating self-sustained state is of central importance in neuroscience, where it is called short-term memory (cf. Ch. 6 in Ref. [13]) or working memory [37]. The excitation "bump" neurocomputational function occurs in models of great current interest, such as place and grid cells [38] and in head direction systems [39]. It also appears in models of the oculomotor system, which allows the gaze to be fixed in a given direction [40].

In a biological neuron, the self-excitatory current may represent the intrinsic transient inward Ca^2+ ionic current, known as I_T (see Ch. 10 in Ref. [13]). If, alternatively, the self-synaptic connection is extrinsic, such as due to the neuron's own axon connecting the dendrites, it is called an autapse, which is a topic of current interest [41–44]. This may be relevant to epilepsy, where it was reported that, in epileptic humans, about 30% of cortical neurons of layer V form autapses [45]. Moreover, very recently, it was observed that the ictal source point of epileptic seizures occurs in layers IV, V, and VI [46].

For a self-excitatory synaptic current, the system of equations (9)–(12) of our model become

$$C_m \frac{dV_m}{dt} = -\frac{V}{R_m[S] + R_a} + I_{\rm sse} + I_0, \tag{17}$$

$$V_{\rm ap} = \frac{V_m}{R_m[S] + R_a} R_a, \tag{18}$$

$$\tau_s \frac{dI_{s1}}{dt} = -I_{s1} + I_\delta H(V_{\rm ap} - \Omega), \tag{19}$$

$$\tau_s \frac{dI_{\rm sse}}{dt} = -I_{\rm sse} + I_{s1}. \tag{20}$$

Here, for the self-excitation, the spike potentials become $V_{\rm pre} = V_{\rm post} = V_{\rm ap}$. Additionally, to indicate the synaptic self-excitatory current, I_{s2} is renamed $I_{\rm sse}$. The system of equations above corresponds to the neurocomputing circuit shown in Fig. 8. The key feature of the activity bump

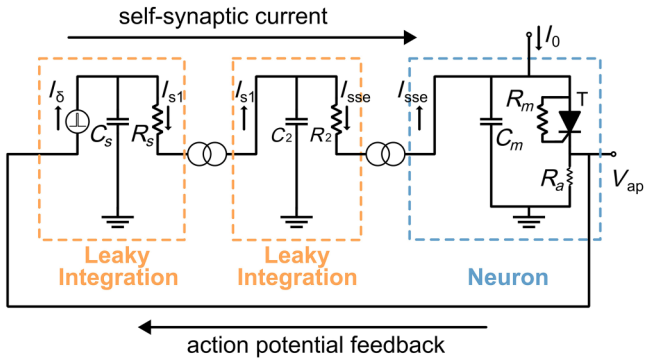

FIG. 8. Self-synaptic current circuit. Here I_0 is the external current input; and V_{ap} is the output train of action-potential spikes. The output spikes are feedback to the neuron through the self-synaptic current I_{sse}.

is that the neuron can reach a spiking state, and remain self-excited, despite the input external current I_0 being *subthreshold*, namely $I_0 < I_{min}$. As we shall discuss below, the self-excitation state is maintained by the buildup of the self-synaptic current I_{sse}.

To start the bump of activity, it is necessary to apply a short excitatory external current pulse I_Δ on top of the constant subthreshold current I_0, as shown in Fig. 9. Since I_0 is subthreshold, we observe that there is no activity during the first 2 s. Then an excitatory pulse is applied, that fulfills two requirements: (i) it has to drive the neuron to the excitatory regime above threshold, i.e., $I_{min} < I_0 + I_\Delta < I_{max}$; and (ii) its duration τ_Δ has to allow for the buildup of the self-synaptic current I_{sse}, i.e., $\tau_\Delta > \tau_s$.

We observe in Fig. 9 that the spiking starts as soon as I_Δ begins, and within the next second $\sim \tau_s$ the I_{sse} starts to build up and the frequency rate increases. Within the next second, by the time I_{sse} is terminated, the self-feedback is well in place. The persistent state is realized as $I_0 + I_{sse} > I_{min}$. The spike rate of the bump of activity stabilizes at the self-consistent rate f^* as we discuss below.

We can recall the two response functions that characterize the neurosynaptic unit (see Fig. 6) and use them to formulate the bump state as a self-consistent problem. On the one hand, we have $f(I_{in})$, the neuron activation function; on the other, the synaptic current $I_s(f)$ that results from the synaptic circuit, given an input spike rate f from a neuron. We should also note from Fig. 9 that $\tau_s > 1/f$, so we are indeed in the rate-coding regime.

We would now like to analyze the dynamical memory state under a different light. We shall show that it can be cast as a self-consistent problem, which can be solved by a geometrical construction. The same method will be used in the next section to consider the case of self-inhibition, i.e., adaptation.

In the self-excitatory motif, the synaptic current is feedback to the neuron, hence $I_s = I_{sse}$ (see Fig. 6). Therefore,

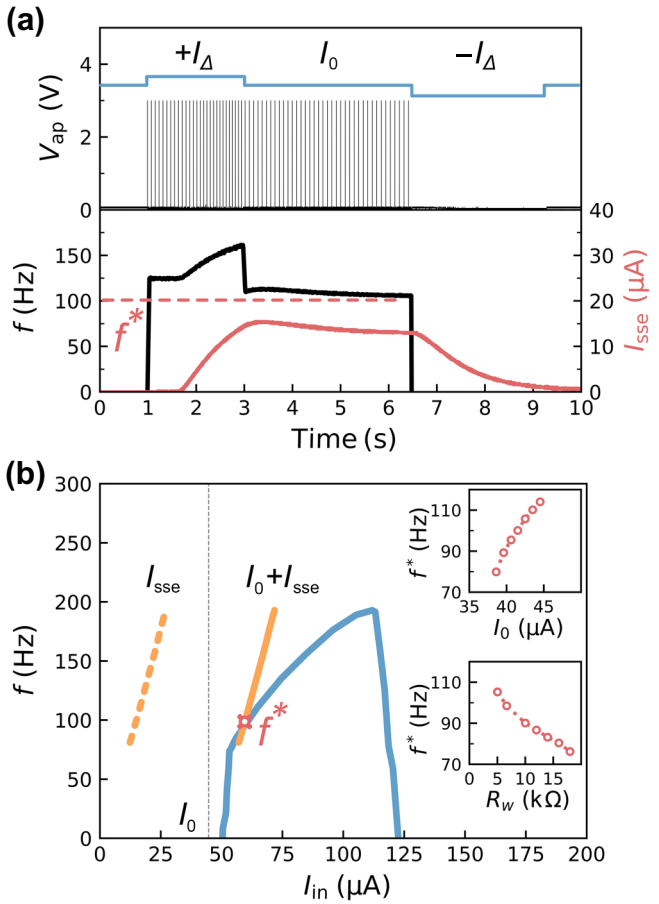

FIG. 9. (a) Top: Spike trace of the excitation bump. The blue line schematically denotes the applied external subthreshold current I_0 with the short excitation I_Δ that starts the bump, and inhibition that terminates it. Bottom: The instantaneous spike-rate emission f of the neuron (black line); and the self-synaptic current I_{sse} buildup during excitation and relaxation during inhibition (red line). The state has an external continuous *subthreshold* $I_0 = 44.7$ μA. (b) Geometrical construction to determine the self-consistent frequency f^*. Insets: f^* as functions of R_W and I_0. The parameters are $\tau_s = 0.47$ s, $I_0 = 44.7$ μA, $+I_\Delta = 22.9$ μA, $-I_\Delta = -24.4$ μA. For clarity, the number of spikes is reduced to one-tenth of the originally measured number.

we can cast the bump as a self-consistent problem: (i) the total input current is $I_{in} = I_0 + I_{sse}[f]$, where I_0 denotes a constant subthreshold external current and I_{sse} is the self-excitatory contribution that depends on the spiking frequency; and (ii) the total I_{in} produces a spike rate $f(I_{in})$, which itself produces the feedback current I_{sse}. Therefore, the problem of simultaneously fulfilling (i) and (ii) is to find the self-consistent frequency f^* such that $f^* = f[I_0 + I_{sse}(f^*)]$.

The solution to this problem can be obtained by a geometrical construction. It corresponds to the crossing point (I^*_{in}, f^*) between the two response functions measured on the NS unit (see Fig. 6). From the first response, we call

$f_1 = f_1(I_{\rm in})$, which is shown by the blue line in Fig. 9(b). From the second response, we invert the variables to get $f_2 = f_2(I_s) = f_2(I_{\rm sse})$, shown in dashed yellow line in Fig. 9(b) (and compare to Fig. 6). From (i) above, we have $I_{\rm in} = I_0 + I_{\rm sse}$; then we get $f_2 = f_2(I_{\rm in} - I_0)$, which is the yellow solid line in Fig. 9(b). The geometrical solution is obtained by requiring $f_1 = f_2$, which gives the crossing point $(I^*_{\rm in}, f^*)$, as shown as a red cross in Fig. 9(b).

We can further explore how the self-consistent firing rate f^* systematically depends on two main parameters of the model, as we show in Fig. 9. One is the synaptic weight R_W, which controls the intensity of the feedback current. This intensity is controlled by the "neurotransmitter" charge Q_N, which is modulated by the synaptic resistor R_W (see Fig. 4 and Sec. II D). The other parameter is the external current intensity I_0, which is always kept subthreshold for the activity bump. One could in principle set $I_0 = 0$ and still realize a bump. The requirement is a strong enough feedback, such that $I_{\rm sse} > I_{\rm min}$. The continuous dependence of the f^* on the model parameters is shown in the insets of Fig. 9(b).

One of the long-standing issues in theoretical models of this type of dynamical attractor concerns their stability with respect to perturbations, since it is based on a positive feedback loop [19,40]. Therefore, it is important to note a conceptual point in this regard. The methodology that we adopt in the present work is based on the *physical* implementation of a theoretical model. Thus, the stability of the dynamical attractor model is directly demonstrated *by construction*. Namely, if it works, therefore, it must be stable. Nevertheless, we may further demonstrate this feature by explicitly applying strong external perturbations to the activity bump state. This is shown in Fig. 10. Despite these strong perturbations, even halting the spikes in the inhibitory case, the dynamical attractor returns promptly to its stable state, as shown in the inset. A key feature for the stability, however, is that the perturbations should not last much longer than the synaptic timescale τ_s. Hence, we may say that this state can keep a short-term memory encoded by f^* during that characteristic timescale.

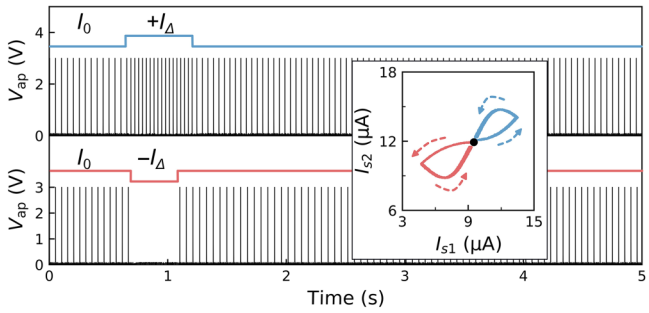

FIG. 10. Stability of the bump attractor state. Top: An excitatory current pulse of intensity $+I_\Delta = 22.9$ μA (blue line) is applied during 1.2 s, producing an increase in the firing rate, which rapidly relaxes after the perturbation stops. Bottom: An inhibitory perturbation $-I_\Delta = -24.4$ μA is applied during 0.8 s, producing a halt on the spiking. The bump recovers rapidly after the perturbation stops. Inset: Evolution of the synaptic currents I_{s1} and $I_{s2} = I_{\rm sse}$ during the perturbation. The parameters are $\tau_s = 0.47$ s and $I_0 = 44.7$ μA. The number of spikes is reduced to one-fifth for the sake of clear display.

Finally, from these stability considerations, it follows that, to stop the active bump state, one needs to apply an inhibitory current pulse $-I_\Delta$ that is sufficiently long and strong. More precisely: (i) its magnitude has to be such that the total input current $I_{\rm in} = I_0 + I_{\rm sse} - I_\Delta < I_{\rm min}$, i.e., falls below the onset of excitability, so stops the firing and allows the feedback to relax; and (ii) its duration, therefore, should be longer than τ_s, such that the self-synaptic current $I_{\rm sse}$ relaxes sufficiently, as shown in Fig. 10, such that the condition (i) is fulfilled.

C. Self-inhibition: Adaptation and bursting

In this section, we turn to another minimal motif, namely that of neuron self-inhibition (see Fig. 7). As we shall see, this motif produces two important spiking modes: adaptation and bursting. These modes will be the basis for the multineuron motif for central pattern generators, which we shall describe later in the next section.

1. Adaptation

Adaptation is a relevant function in neuroscience. An example of this type of self-inhibition is the after-hyperpolarization current I_{AHP}, which is mediated by Ca^{2+} (see Ch. 10 in Ref. [13]). Similarly, as mentioned in the previous section, this motif may also be realized by an external connection between the neuron's own axon and its dendrites. This case is called an inhibitory autapse, which is now known to be a common feature of some neocortical and parvalbumin (PV) neurons, with the function of regulating the rate of spike emission [42,45,47,48]. Self-inhibition is also a main ingredient of two of the most popular schematic theoretical models, Izhikevich and AdEx [3,17]. In both models, the self-inhibition is described by a second dynamical equation for the adaptation or recovery variable.

Similarly as done in the previous section, we shall also show how the spiking states of this motif can be cast as a self-consistent problem. The geometrical solution of the self-consistent problem brings valuable insights, specially for the understanding of the stability of the firing states and the nature of the bursting one. Rather surprisingly, despite a very large literature on the Izhikevich and AdEx models, we are not aware of any similar treatment to the one we introduce here [3]

We first begin by exploring the dynamical behavior of this important motif by means of our hardware implementation. In this case, the system of equations (9)–(12) of our

theoretical model becomes:

$$C_m \frac{dV}{dt} = -\frac{V}{R_m[S] + R_a} - I_{\rm ssi} + I_0, \tag{21}$$

$$V_{\rm pre} = \frac{V}{R_m[S] + R_a} R_a, \tag{22}$$

$$\tau_s \frac{dI_{s1}}{dt} = -I_{s1} + I_\delta H(V_{\rm ap} - \Omega), \tag{23}$$

$$\tau_s \frac{dI_{\rm ssi}}{dt} = -I_{\rm ssi} + I_{s1}. \tag{24}$$

Here we now need to excite the aLIF neuron with a *suprathreshold* external current I_0, unlike in the previous section. Also, we rename the synaptic current I_{s2} as $-I_{\rm ssi}$ to denote the synaptic self-inhibition. The circuit configuration is identical to that shown in Fig. 8 for the self-excitation, with the sole difference that the mirrored current I_{s2} is now of inverted polarity.

While it is possible to have some degree of adaptation in the spike-by-spike regime, when $\tau_m > \tau_s$, the most natural, interesting, and biologically relevant case is the rate-coding regime, i.e., for $\tau_m \sim 1/f \ll \tau_s$. Hence, we focus here on the latter. In Fig. 11 we show the behavior of the aLIF with a self-adapting current. The adaptation results from the buildup of the inhibitory current intensity $I_{\rm ssi}$ on the synaptic subcircuit, which occurs within the synaptic timescale τ_s. The total current exciting the neuron gets reduced to $I_{\rm in} = I_0 - I_{\rm ssi}$, which leads to the reduction of the firing rate with respect to the original one, $f\,(I_0)$. This phenomenon of spiking rate reduction is called frequency adaptation.

As we did before, we may also consider this state as a self-consistent problem, where we need to find the spike rate f^*. Now, the self-consistent condition is given by $f^* = f^*(I_{\rm in}) = f^*[I_0 - I_{\rm ssi}(f^*)]$. As we discussed before, in Sec. II D, Eq. (16), the response function $I_{\rm ssi}(f) \approx -Q_N f$, i.e., identical to the response function $I_{\rm sse}(f)$ with a change of sign. So the inhibitory current represents a discharge of C_m.

In Fig. 11 we show the geometrical construction for the case of a negative self-synaptic current, which follows the same steps outlined before. Similarly, as in the case of self-excitation, the self-consistent frequency can be controlled by modulating the intensity of the feedback current. This can be achieved by varying the model parameters, such as R_W and I_0, as shown in the insets of Fig. 11.

Also similarly as done before for the bump, the stability of the adapted self-consistent state can also be tested by applying perturbations. Our results are shown in Fig. 12, where we demonstrate very good stability.

Before leaving this section we should make a final point. As already mentioned before, it is one's choice to adopt one or two leaky integration blocks. This choice can be made in either the excitatory or the present inhibitory case.

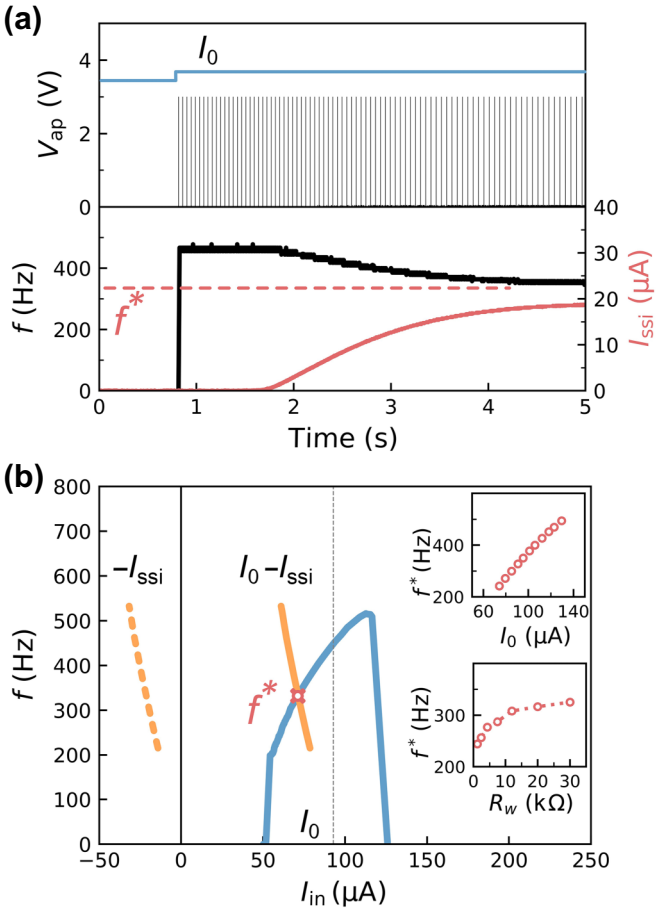

FIG. 11. Adaptation traces. (a) Top: Spiking trace showing the progressive reduction of the frequency. The blue line indicates the external current input $I_0 = 92.8$ μA. Bottom: The instantaneous spike rate f. The red line shows that the self-synaptic adaptation current $I_{\rm ssi}$ builds up over a timescale $\tau_s \approx 1$ s; and f^* denotes the self-consistent asymptotic frequency. (b) Geometrical construction to determine the self-consistent frequency f^*. Insets: f^* as functions of R_W and I_0. The number of spikes is reduced to one-twentieth for the sake of clear display.

Below, we explicitly write the model equations, where we adopt the simplified notation of Eq. (1), for the sake of clarity, and adapt them for the case of one inhibitory leaky integration stage. The system reads

$$C_m \frac{dV_m}{dt} = f\,(V_m) - I_{\rm ssi} + I_0, \tag{25}$$

$$\tau_s \frac{dI_{\rm ssi}}{dt} = -I_{\rm ssi} + I_\delta H(V_{\rm ap} - \Omega). \tag{26}$$

The reader may verify that these equations now share the same form as the Izhikevich and AdEx models [3,17]. The I_δ term represents the spikes due to the action potentials $V_{\rm ap}(t)$, which are analogous to the potential spikes of fast variable $V(t)$ in the theoretical models. In all cases, these

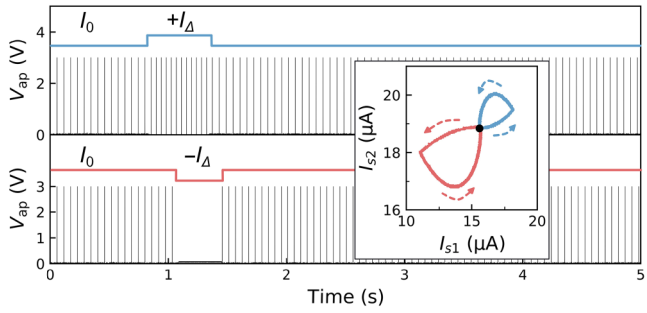

FIG. 12. Stability of the frequency-adaptation state. Top: An excitatory perturbation current pulse of intensity $+I_\Delta = 22.6\,\mu$A (blue line) is applied during a short period. This produces an increase in the firing rate, which rapidly relaxes after the perturbation stops. Bottom: An inhibitory perturbation $-I_\Delta = -24\,\mu$A (red line) is applied, producing a halt on the spiking. The adapted state recovers rapidly after the perturbation stops. Inset: Evolution of the synaptic currents I_{s1} and $I_{s2} = I_{\rm ssi}$ during the perturbation. The parameters are $\tau_s = 1$ s and $I_0 = 92.8\,\mu$A. The number of spikes is reduced to one-twentieth for clarity.

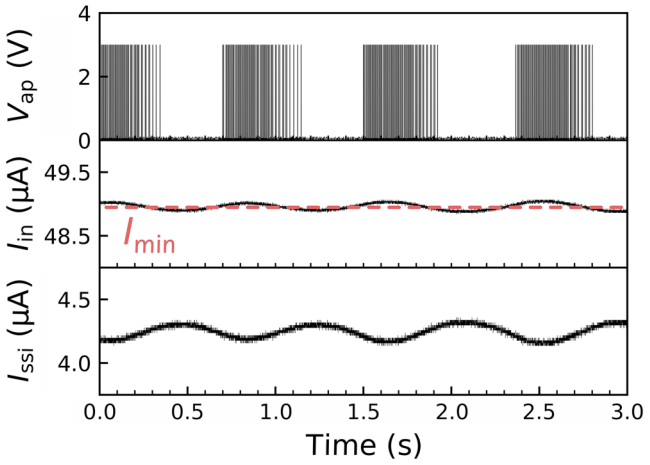

FIG. 13. Burster or pacemaker state. Top: Spike traces showing bursts of activity separated by quiescent states. Middle: The total input current $I_{\rm in}$ is oscillating narrowly around the threshold $I_{\rm min}$. Bottom: The self-inhibitory current $I_{\rm ssi}$ resembling a harmonic oscillation with period $\approx \tau_s = 1$ s, as discussed in the text.

spikes are identically leaky integrated by the recovery variable.

2. Bursting

We have adopted the intuitive perspective of considering states as the solution of self-consistent problems. Therefore, it is interesting to pose the following question: What would happen if we increase the intensity of the adaptation, so that the resulting total input current to the neuron falls below the excitability threshold? Namely, $I_{\rm ssi}$ is such that $I_{\rm in} = I_0 - I_{\rm ssi}(f) < I_{\rm min}$, so that the strong self-inhibition would stop the firing, hence the self-consistent solution is no longer possible.

Let us analyze what would be the expected behavior. The self-inhibition takes a time τ_s to build up and stop the firing. However, this quiescence provokes the relaxation decay of the feedback current, within a timescale τ_s. Recalling that $I_0 > I_{\rm min}$, the total input $I_{\rm in} = I_0 - I_{\rm ssi}$ will grow as $I_{\rm ssi}$ decreases and, eventually, the neuron will get re-excited and start spiking again. Thus, this dynamical bistability points to periods of spike emission alternating with quiescent ones. Such a state is called bursting, which is another basic neurocomputing primitive of the self-adaptation motif.

The bursting state is implemented by the NS unit as we show in Fig. 13. From the qualitative discussion, it should be clear that the bursting state is controlled by the two timescales τ_m and τ_s. The latter controls the alternation period or burst cycle, and the former the interspike intervals during each burst. Hence, we have $\tau_m \ll \tau_s$ so the neuron is in the rate-coding regime. Moreover, from the previous discussion, one should expect that the intraburst spiking frequency has to evolve around the excitability threshold $I_{\rm min}$. As shown in Fig. 13 this is indeed the case, with $I_{\rm ssi}$ oscillating around the threshold $I_{\rm min}$ within a fraction of a μA.

We may gain further and deeper analytic understanding of those small oscillations. This is revealed by a simple analysis of the model equations, which to our knowledge has not been done before. We consider the model equations and take the time derivative of Eq. (24) and replace it into Eq. (23) to obtain

$$\tau_s^2 \frac{d^2 I_{\rm ssi}}{dt^2} + 2\tau_s \frac{dI_{\rm ssi}}{dt} + I_{\rm ssi} = I_\delta[f\,(t)]. \tag{27}$$

This differential equation is the analogue to the familiar driven damped harmonic oscillator model [49] with resonant frequency $1/\tau_s$. The "friction" or damping is the second term and the "external driving force" is $I_\delta[f\,(t)]$. From the behavior of this well-known system, we may expect two different states: one where the damping dominates, and another where the oscillations persist. Indeed, as shown in Fig. 13, the synaptic current $I_{\rm ssi}(t)$ exhibits a beautiful oscillatory behavior with a period close to $\tau_s = 1$ s, as predicted by Eq. (27).

However, our driven damped oscillator has a twist, since the driving force is not arbitrary but depends on the neuron's spiking trace through the feedback loop. So we can discuss the nature of the oscillation in more detail. Let us assume that the system is bursting and show that this assumption is consistent. The current $I_\delta[f\,(t)]$ consists of trains of fast spikes at frequency f separated by silent periods, thus having a rhythmic time dependence with period τ_s. The trains of current spikes are twice leaky integrated with timescale τ_s; therefore, $I_{\rm ssi}(t)$ builds up within the

same timescale as the period. Similarly, during the quiescent phase, the inhibitory current relaxes on the same timescale. Then, the periodic buildup and relaxation of $I_{\rm ssi}(t)$ modulates the firing behavior of $f\,(t)$, hence of I_δ, and the bursting state is consistent. The point to make is that the "driving force" $I_\delta(t)$ is in resonance, as the trains of spikes are emitted at a frequency $1/\tau_s$, which is the natural frequency of the oscillator equation (27). Within the same line of reasoning, the simple adaptation can be understood as an overdamped oscillation.

IV. CENTRAL PATTERN GENERATORS

We are now ready to start building general functional spiking neural networks. We shall begin by considering the simplest multineuron motif, namely two neurons coupled by dynamical synaptic currents [20]. We shall focus on implementing an SNN whose neurons emit periodically alternating bursts. Such a two-neuron network is called a central pattern generator and has a very important role in neuroscience [32]. This type of spiking activity is fundamental for motor systems with periodic dynamics, such as heartbeats, walking, eating, etc. Moreover, CPGs are also a key component in robotics, self-propelled systems, and biomedical devices. Therefore, our simple and systematic methodology may open an interesting avenue for applications. We want to emphasize here that the methodology of combining motifs is general. One can go on combining motifs in a modular manner to achieve more complex spiking behaviors, such as, for instance, the classic problems of gaits and swimming [35]. A technical side remark is to realize here that the formulation of our circuit models is done in terms of currents and implemented by current sources and current mirrors. Unlike voltages, input current sources can be added algebraically.

The CPGs involve an external excitation that induces the basic tonic spiking of each neuron, which is then sculpted by inhibitory synaptic currents acting on different timescales. As this is a vast field, we shall adopt the review of Marder and Bucher [32] as guidance to select a few paradigmatic systems to build. Nevertheless, in doing that, we shall also obtain insights provided by the present hardware-based approach.

We shall consider three different basic CPGs [32] that correspond to two different two-neuron motifs, those in Figs. 7(d) and 7(e). One has primary-subordinate or feedforward inhibition architecture, while the other has recurrent connections of mutual inhibition. In the model circuits here, we adopt all synaptic currents, intra- and interneuron, as inhibitory $\alpha(t)$-type functions.

1. Primary-subordinate CPG

We start with the simplest case, the motif in Fig. 7(d). Such CPG has a bursting neuron (N1), acting as a pacemaker, that sculpts the firing rate of a regular spiking neuron (N2) by projecting inhibition. The pacemaking neuron is realized by a bursting neuron, as discussed in the previous section. The subordinate neuron shows regular spiking when uncoupled, as shown in Fig. 14. When the inhibitory projection is introduced, the subordinate neuron develops a burst spiking pattern that is the inverse of its primary's (see Fig. 14). Hence, the two-neuron system displays a sequence of alternating bursts which is characteristic of CPGs.

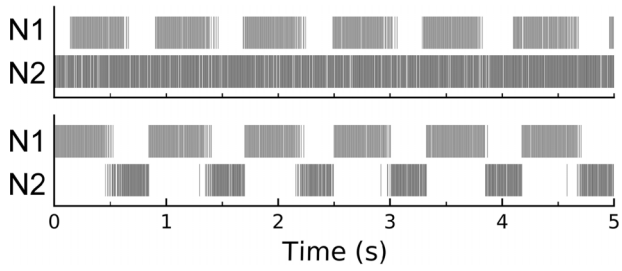

FIG. 14. CPG primary-subordinate. Top: Uncoupled case, in which N1 is a pacemaking burster and N2 is a regular tonic spiking neuron. Bottom: Coupled case, in which the N2 subordinate is inhibited by the activity of N1, creating a complementary bursting pattern. Parameters are $\tau_{\rm ssi} = 1$ s for the pacemaking and $\tau_{\rm spi} = 1$ ms for the fast inhibitory projection.

A requirement to achieve this state is that the interneuron synaptic projection from the primary has to be strong enough to silence the subordinate, i.e., to drive the subordinate under its excitation threshold. So for the currents acting on N2, we have

$$I_{\rm in} = I_0 - I_{\rm spi} < I_{\rm min} \tag{28}$$

where $I_{\rm spi}$ denotes the synaptic projected inhibitory of N1 on N2. The intensity of the projection can be easily controlled by the resistance R_W of the $I_{\rm spi}$ synaptic circuit.

2. Mutual-inhibitory CPG

We turn now to the second motif, with mutual inhibition. In this case, we shall consider two qualitatively different possibilities: two coupled bursters and two coupled adaptive neurons. For simplicity, we shall consider symmetric systems. However, it is important to acknowledge that inherent variability exists in all hardware as a result of manufacturing tolerances. Nevertheless, as with biological neural neurons that are also nonidentical, the emergent function has to be robust to that type of variability.

Two mutually coupled pacemakers present a more straightforward case; therefore, we begin our discussion with this scenario. We consider two neurons that, if decoupled, both produce the same bursting (cf. Sec. III C 2), up to the intrinsic variability just mentioned. Therefore, the actual observed behavior is of two similar, but not identical, periodic burstings, as shown in Fig. 15. By introducing

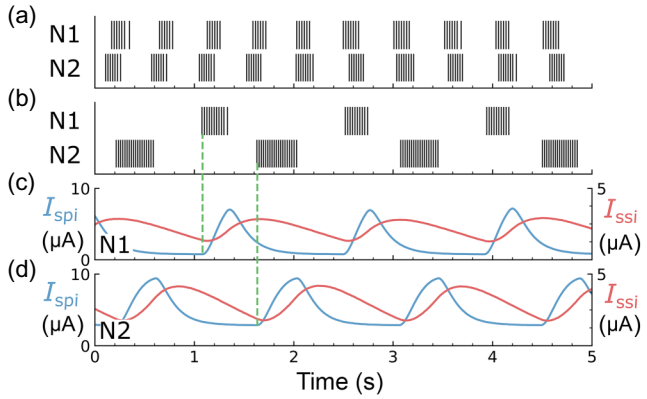

FIG. 15. CPG mutual inhibitory pacemaker. (a) Uncoupled case: N1 and N2 are pacemaking bursters with nominally equal, but in practice similar, frequencies. (b) Coupled case: N1 and N2 settle into a common antisynchronous bursting pattern. (c) Synaptic currents of N1: the self-inhibitory I_{ssi} with $\tau_{ssi} = 0.47$ s (red) and the N1 to N2 projected inhibition I_{spi} with $\tau_{spi} = 0.1$ s (blue). The green line marks the beginning of an N1 burst. (d) The same as panel (c) but for the synaptic currents of N2. For clarity, the number of depicted spikes is reduced by one-fifth of the originally measured number.

coupling in the form of projection of mutual inhibition [see the motif in Fig. 7(e)], we create anticorrelation in the respective firing patterns. As we can see in Fig. 15(b), the state of the two-neuron network finds a compromise where they burst in antiphase. Therefore, they both lock into a single common frequency. This emerging frequency is close to the uncoupled ones, but relatively reduced due to the global effect of additional inhibition.

In this case, it is interesting to observe the synaptic currents, which we show in Fig. 15. They bring interesting insights. Following the green dashed line we can correlate the burst of each neuron with the respective effects on their synaptic currents. The first thing to realize is that the burst induces $\alpha(t)$-type currents, which can be clearly appreciated. The maximum of $\alpha(t)$ indicates the respective time constants, which we denote $\tau_{ssi} = 0.47$ s and $\tau_{spi} = 0.1$ s for synaptic self-inhibitory (red) and synaptic projected-inhibitory (blue).

If we focus on the synaptic currents of N1, shown in Fig. 15(c), we can see that the burst starts when the self-inhibitory I_{ssi} decreases to almost its lowest intensity. Conversely, the burst is terminated shortly after due to the buildup of I_{ssi}, i.e., occurring within a timescale somewhat shorter than τ_{ssi}. On the other hand, we observe that the antisynchrony is due to the strong inhibitory projection, which has a relatively faster timescale τ_{spi} and prevents the superposition of bursts. Similar considerations can be made for the other neuron's currents. We can also observe that the different initial traces in the two decoupled neurons [Fig. 15(a)] also reflect some differences in the respective produced currents. Nevertheless, the two neurons robustly lock to a common and stable pattern of alternated bursts.

It would be interesting, but beyond the scope of the present study, to perform a full exploration of the different emergent states of the two coupled bursters. Nevertheless, we can now qualitatively discuss some relevant aspects regarding the relative timescales.

In the case discussed above, we note that the duration both of the bursts and of the projected inhibition τ_{spi} are relatively short, leading to the antisynchrony already discussed. However, one may choose to increase τ_{spi}, so that it is significantly longer than the bursts. Then the projection from, say, N1 to N2 will be delayed compared with the burst in N1. This projected inhibition would make the burst of N2 in antisynchrony less likely. The result is that the emergent state would be that of synchrony between N1 and N2. This situation is qualitatively similar to that analyzed by van Vreeswijk *et al.* [20] for the case of two simple spiking neurons coupled by a retarded mutual inhibition.

We may finally turn to another, more subtle, form of CPG, which shares the same motif as in Fig. 7(e), but is found in a different regime. This CPG is realized with two neurons that exhibit spike-frequency adaptation, i.e., are tonic spiking when uncoupled (cf. Sec. III C 1). This type of CPG model is a classic topic of neuroscience, as it finds a biological realization in the heartbeat neural activity of the leech [33,34,50].

The behavior of this mutually adaptive CPG is shown in Fig. 16. It also shows alternate burst emission, but with a different mechanism. We note that, for illustrative purposes, we have maintained the synaptic time constants the same as in the previous case. The present mechanism is achieved by mainly driving N1 and N2 to the adaptation regime, reducing the intensity of the self-inhibition (see Sec. III C 1).

As seen in Fig. 16 the CPG traces show qualitative differences with respect to the previous case. One is that the burst shows some overlap. Also in contrast to the previous case, we can now observe a significant frequency modulation, where $f(t)$ decreases at the onset and the termination of the burst. This modulation is correlated to the total input current $I_{in}(t)$, which shows a similar behavior. Note that it crosses the excitability threshold I_{min} as it produces the bursts.

To appreciate the mechanism, it is essential to look at the synaptic currents generated by each neuron. They are shown in Figs. 16(e) and 16(f). As before, in red is the self-inhibition I_{ssi}, and in blue is the projected inhibition to the other neuron I_{spi}. The green dotted lines are a guide to indicate the beginning and end of the burst of N1. The analysis for N2 would be the same.

We focus on the start of the burst of N1. We observe that its self-inhibition I_{ssi} is decreasing towards its minimum [red line in Fig. 16(e)], similarly as in the CPG case discussed before. However, unlike that case, now N2 is firing

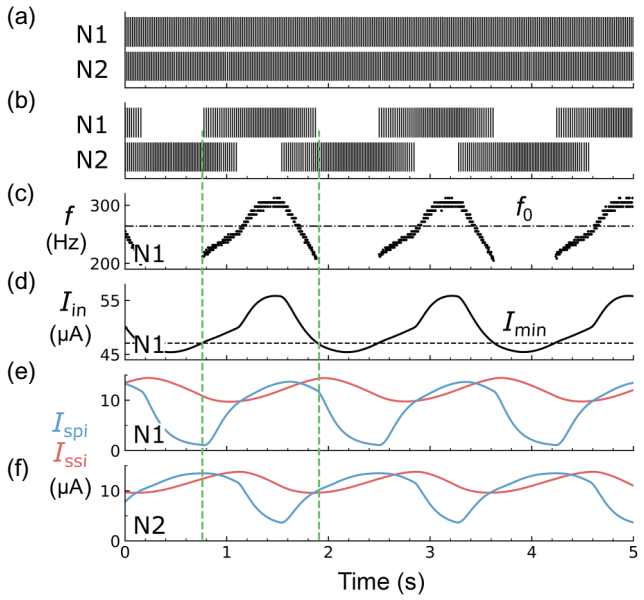

FIG. 16. CPG mutual inhibitory adaption. (a) Uncoupled case: N1 and N2 are adaptive neurons with tonic spiking. (b) Coupled case: N1 and N2 settle into a common antisynchronous bursting pattern. (c) The instantaneous frequency rate of N1. The green lines denote the beginning and end of a burst. The horizontal dashed-dotted line indicates the adapted frequency f^* when the neurons are decoupled. (d) Total input current $I_{\text{in}}(t)$ to N1. The beginning and end of the burst coincide with the crossing of the excitation threshold I_{min}. (e) Synaptic currents of N1: the self-inhibitory I_{ssi} with $\tau_{\text{ssi}} = 0.47$ s (red) and the N1 to N2 projected inhibition I_{spi} with $\tau_{\text{spi}} = 0.1$ s (blue). (f) The same as panel (e) but for the synaptic currents of N2. For clarity, the number of depicted spikes is reduced by one-fifth of its original measured number.

and intensively projecting its inhibition I_{spi} on N1 [blue line in Fig. 16(f)]. In consequence, the reason why N1 starts to fire is only due to the decrease of its self-inhibition. We may say that N1 recovers and escapes from the grip of N2. This is one of the four typical CPG mechanisms, and is indeed called "intrinsic escape" [23,51].

We may also look at the end of the burst phase. There we observe that both I_{ssi} and the received projection I_{spi} are on the rise, so they both contribute to inhibiting N1. Moreover, the projection of N2 is *necessary* to increase the inhibition of N1 and render it quiescent. This is because N1 is now an adaptation neuron and not a pacemaker as in the previous case.

This last observation is relevant because it explains an evident qualitative difference between the patterns of the two modes of CPG that we considered. By comparing the spiking traces of Figs. 15 and 16, we observe that, in the first case, the bursts do not overlap in time, while in the second they do. The reason is that, in the first case, the ability to burst is an intrinsic feature of each neuron, while the inhibitory projection solely creates an anticorrelation between them and lengthens the period. In contrast, in the second case, the neurons do not have the pacemaking ability to quiet themselves. Thus the overlap of activity is a *necessity*. This qualitative difference is a robust feature that may help in the classification and understanding of CPGs in biological systems. For instance, the heartbeat of the leech is a classic CPG animal model and is a clear example of overlapping bursts [50]. On the other hand, the CPG of the stomatogastric ganglion of crustaceans, which is another paradigmatic animal model, is a clear example of pacemakers with anticorrelations [32].

V. DISCUSSION: EXTENSIONS TO OXIDE MEMRISTORS AND TO VLSI

A. A template for memristive material research

In this work, we have introduced a circuit implementation of a general-purpose, theoretically based, neurosynaptic model using solely conventional electronic components. This has the evident advantage that the methodology can be easily reproduced at a very affordable cost and wide availability.

Nevertheless, our methodology also opens an exciting perspective for researchers in material science working on memristive systems. In fact, our circuit can be adopted as a template for testing memristive devices and building small to midscale functional networks. More specifically, there are two places where memristors may find their place. The first one is in the neuron stage. There, the memristor device (thyristor plus resistor) can be replaced by a *volatile* oxide memristor, such as VO_2, V_2O_3, V_3O_5, $NdNiO_3$, $SmNiO_3$, NbO_2, etc. [26,52–56].

The synaptic resistance R_W is the second place where an oxide memristor, which should now be a *nonvolatile* memristive material, can replace a conventional resistor in our NS-unit circuit. The R_W resistance controls the intensity of the synaptic coupling W_{ij} between two neuron units i and j, in the language of artificial intelligence systems. Nonvolatile oxide memristors such as TiO_2, Ta_2O_5, HfO_2, etc., are popular choices for synaptic cross-bar neuronal networks [26,57]. The plasticity in the resistance modulation of oxide memristors may further endow the network with learning ability [58].

B. Positioning and comparison to other neuromorphic hardware

A lot of overlap and confusion exist in the field of hardware-based neuromorphic systems. So we may first distinguish our approach by enumerating what our system is not: (i) It is not based on transistors in the subthreshold regime, as CMOS chips are. Thus, it is much less affected by the variability mismatch issue. (ii) It is not based on digital hardware, which is not well adapted for the continuous nonlinear dynamics of excitability characteristic of spiking

systems. (iii) It is not based on memristive oxide systems, which are still under research in the realm of material science. (iv) It is not based on software simulations on neuromorphic digital chips, such as field-programmable gate arrays (FPGAs), Loihi, etc., which present the issue of matching biological timescales [34].

On the other hand, we should also enumerate what our system is: (i) It is a novel hardware implementation of a textbook set of equations [13] of a general spiking neurosynaptic model. (ii) It is implemented with elemental electronic circuitry (see the Appendix). (iii) It is implemented in a clear, direct, and quantitative manner, where every model parameter has a hardware correlate enabling full tunability (see Sec. II C). (iv) Its electronic components are widely available and economic, so our system can be immediately duplicated and the data reproduced (see the Appendix). (v) It provides a direct hardware implementation with continuously tuned and biocompatible timescales (see Sec. IV), so it is ready to be deployed for applications in robotics, medical devices, control systems, etc.

We would now like to comment on the size of the SNNs that we may reach with the present methodology. The limitations do not come from fan-in and fan-out, which are essentially unconstrained. This is because we formulated all our models in terms of currents which can be added at the input of neurons. Thus the limitations are due mainly to the practical size of the systems that one may want to implement. We can estimate this on the order of hundreds of units, or maybe more for simple architectures. This should be sufficient, not only for the applications mentioned above, but also for research in theoretical neuroscience. In fact, it is now increasingly recognized that the dynamics of biological neural systems can often be described in low-dimensional manifolds.

While the present approach is qualitatively different than those based on VLSI, we should mention that it can be ported to VLSI, if it is so desired. In fact, the implementation of the memristive neuron unit has already been reported [59], where the function of the thyristor was emulated by two transistors. On the other hand, the synaptic unit is based on current mirrors, which are standard to VLSI. A single stage of a leaky-integration synapse has already been implemented some time ago [12,60]. So, the present improvement based on a two-stage integration that implements Rall's function should not present any significant impediment.

Nevertheless, it is important to emphasize that two main features would still distinguish the present methodology from previous VLSI approaches. First, and more important, our neuron circuit design would likely suffer less from device mismatch, since it is based not on subthreshold behavior but on the memristive effect [59]. Second, there is the higher simplicity of our circuit designs.

Another important aspect that needs to be commented upon is the power efficiency. While the present work is not focused on engineering aspects, this feature is relevant for eventual practical applications. The main qualitative difference from current VLSI implementations is, of course, the size of the components. One may naively assume that the miniaturization of VLSI may have a dramatic impact on power consumption. However, this is not the case. The energy cost per spike can be estimated as proportional to CV_{th}^2, where C is the capacitance of the membrane capacitor and V_{th} is the threshold voltage for spike emission. In VLSI, the miniaturization implies small values of C, but it also implies high spike frequency rates. In fact, the energy per spike is proportional to C, but the frequency is inversely proportional to it. Therefore, the electrical power (energy of a spike times the spiking frequency) becomes independent of C, hence miniaturization has no effect. On the other hand, our bottom-up method can use a smaller number of spiking units compared to VLSI, which needs to average populations of neurons to mitigate the mismatch [15]. Thus, achieving the same function with a dramatically smaller number of units does imply lower power requirements for our approach.

To compare the power efficiency with digital computers is less easy to establish. A practical possibility to address this question would be to compare the implementation of our CPGs with that achieved using FPGAs [34]. This is an interesting issue to address, which lies beyond the scope of the present work.

VI. CONCLUSIONS

In the present work, we have introduced a novel neurosynaptic device that is the building block of a methodological platform to implement general spiking neural networks with a bottom-up approach. More specifically, we introduced a synaptic unit with biomimetic dynamics that, combined with our previously introduced spiking neuron [27,28,61], completes a platform to build arbitrary SNNs in hardware.

We illustrated the advantages of the approach by considering several basic motifs of theoretical neuroscience, whose dynamics has already produced results and insights.

Firstly, we found that a dynamical memory can be implemented with just one recursive spiking neuron, in contrast to the common wisdom that a population is required. The stability of the memory state is validated explicitly by the methodology that is based on measurements done on hardware implementation.

Secondly, we introduced a model of self-adaptation, similar to Izhikevich or AdEx, but where we adopt a more biomimetic form for the adaptation variable, given by the Rall's function [3]. In that model we found an unexpected analogy between the bursting state and the oscillations in a paradigmatic dynamical system of physics, the driven harmonic oscillator.

Thirdly, we showed that the problem of recursive motifs can be cast as a self-consistent problem where we provided a geometrical solution. This may open the way for progress in the understanding of spiking neurons with recursion.

In addition, from a neuromorphic electronic systems perspective, our approach has a number of innovations and advantages with respect to more conventional ones based on VLSI systems.

(1) Our synaptic circuit model introduces a novel double-step leaky integration which implements a realistic biomimetic dynamical function. It introduces a delay, which, from theoretical neuroscience, is known to be crucial to capture phenomena such as synchrony with inhibitory couplings [20].

(2) Our bottom-up methodology trades miniaturization for tunability and flexibility, hence it can be naturally made to work at biorealistic timescales. That feature is an important drawback in CMOS VLSI, whose miniature capacitors imply bioincompatible high spike rates.

(3) Our methodology provides an explicit way to avoid the mismatch problem that plagues VLSI subthreshold systems and prevents their practical adoption [15]. In contrast, our circuits are built around thyristors, thus less affected by mismatch. Moreover, using discrete components, one may achieve any desired level of device homogeneity by simply performing presorting.

(4) Our methodology is simple and of extremely low cost and availability, hence it may be immediately reproduced and widely adopted. Moreover, our SNN circuits produce robust electric signals, making it an ideal platform for the implementation of a large range of practical applications. Those systems may range from biomedical devices, such as deep brain stimulation, through reservoir computers, and neuroscience instrumentation, to central pattern generators for locomotion, and many others.

Finally, the present approach opens two exciting perspectives ahead: It may finally unlock the promise of neuromorphic electronics for artificial intelligence devices, as it provides a simple and widely accessible modular platform to build hardware devices. Also, it may provide a path to construct a general-purpose SNN simulation machine based on a sound theoretical model for research in neuroscience, beyond what can be done with software running on digital computers.

ACKNOWLEDGMENTS

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APPENDIX

Here we provide details on the circuit implementations of our NS unit. We shall describe each block in detail, and give lists of materials for them along with manufacturer (Manuf.) in Tables I and II. We also provide the values of all components used in the different figures at the end, in Table III.

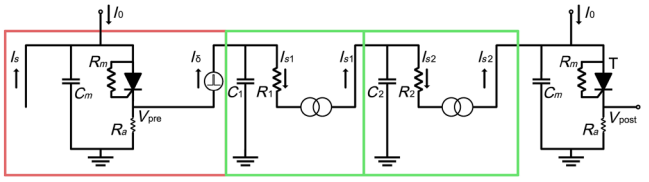

FIG. 17. Details of the neurosynaptic unit circuit blocks. The neuron block is in the red box, while the blocks of two synaptic stages are in the green boxes.

While the circuits can be easily implemented in breadboards, we also supply the printed-circuit-board (PCB) designs along with a list of components in github [62].

In Fig. 17 we reproduce the schematic circuit of Fig. 3, where we have now split the circuit into slightly different modular blocks. The convenience of this should be evident, as the two green blocks are identical. Moreover, with this partition, the system is fully modular. For instance, one may construct a network of neurons that communicate $\delta(t)$ spikes without any delay by combining the red neuron blocks. Alternatively, one may just add one green block at the output of the preneuron to implement $\exp(-t/\tau_s)$ synaptic current coupling. One may also add

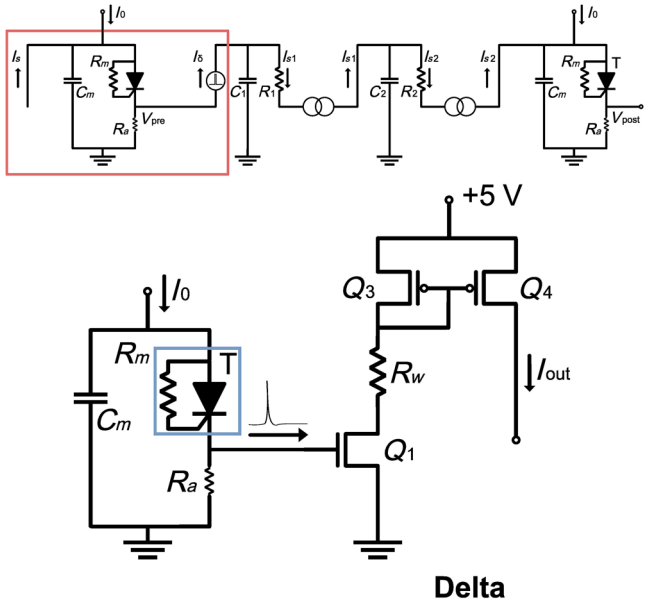

FIG. 18. Schematic of the neuron plus I_δ current block. The Q_1, Q_3, and Q_4 are CMOS transistors from the ALD1105PBL chip. The memristor that implements the voltage-gated conductance channel of the axon hillock is implemented with a thyristor (STMicro P0118MA) with R_m connected between the anode and the gate (blue box). The action-potential spike voltage V_{ap} results from the fast discharge of C_m on R_a when the memristor is in the low-R state.

TABLE I. List of materials for the neuron plus I_δ block.

Component	Manuf.	Manuf. no.	Number
Thyristor	STMicro	P0118MA	1
Capacitor	Nova	CCC-52	1
Resistor	Nova	CBR-11	2
MOSFET	ALD Inc.	ALD1105PBL	1
Trimmer resistor	Bourns	3296P-1-203LF	1

TABLE II. List of materials for the excitatory and inhibitory synaptic current circuit block.

Component	Manuf.	Manuf. no.	Number
MOSFET	ALD Inc.	ALD1105PBL	1
Capacitor	Nova	CCC-52	1
Resistor	Nova	CBR-11	1

two green blocks, as in the schematic circuit, to implement the $\alpha(t/\tau_s)$ synaptic coupling. Another important feature, as we shall show below is that the last green block has two further options: one may implement an excitatory or an inhibitory synaptic current, both of either $\exp(-t)$ or $\alpha(t)$ type.

1. Neuron block

The excitatory part of the neuron circuit has been implemented in Ref. [28]; here we add the synaptic coupling. The circuit is illustrated in Fig. 18. The voltage spikes are produced on the "axon hillock" resistor R_a. That voltage spike needs to be transformed into a strong current impulse so one upstream neuron is able to excite, i.e., to drive spikes on a downstream neuron. Moreover, the intensity of the current needs to be modulated so as to realize the synaptic weights W_{ij} between the two neurons i and j. The components to replicate the circuit are listed in Table I.

This is implemented through a simple solution, adopting a conventional current source configuration taken from the data sheet of the ALD1105PBL chip (which has two matched pairs of CMOS transistors).

The output synaptic current is $\delta(t)$-like, and is implemented by a rectangular pulse of current with an intensity controlled by R_W. In the range of interest $I_{\text{out}} \approx 200\ \mu\text{A}$, i.e., well within the excitatory current interval, it can be approximated by $I_{\text{out}} \approx 4V/R_W$. An important point to make is that R_W can be replaced by a nonvolatile memristor in the implementation of learning neuronal networks.

The duration of the rectangular pulse is controlled by the condition $V_{\text{spike}} > \Omega \approx 0.7$ V, i.e., when the spike overcomes the synaptic threshold Ω (cf. Eq. (11) in the main text).

We can estimate some typical values to see that our neuron circuit can easily match biocompatible timescales. The duration of a spike is easily estimated, as it is directly given by the discharge timescale of C_m on the axon hillock resistor R_a. For typical values $C_m = 1\ \mu\text{F}$ and $R_a = 1\ \text{k}\Omega$, we obtain $\tau_a = 1$ ms, which is a typical biological timescale.

We adopted the STMicro P0118MA thyristor, which has a trigger current $I_{GT} \approx 2\ \mu\text{A}$. From this value and the leaky-integration time constant τ_m, we can obtain an approximate expression for the firing rate for a constant input current I_0. The capacitor C_m charges approximately

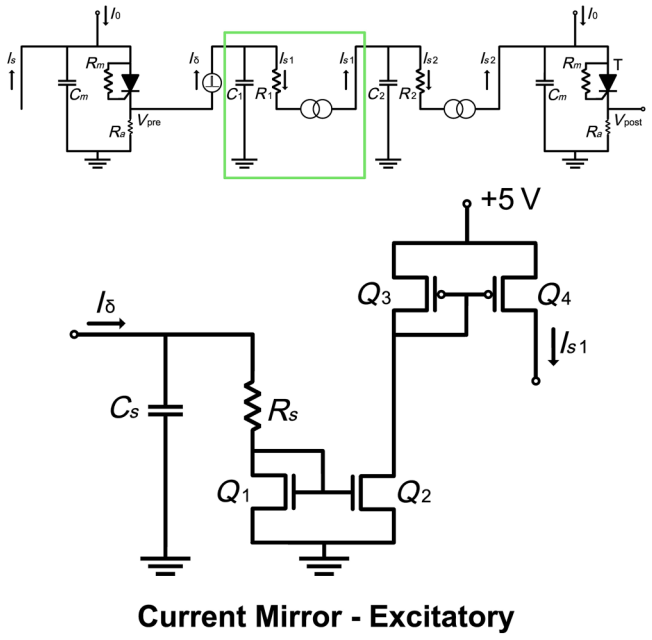

FIG. 19. The excitatory synaptic current circuit block. Here Q_1, Q_2, Q_3, and Q_4 are CMOS transistors from the ALD1105PBL chip.

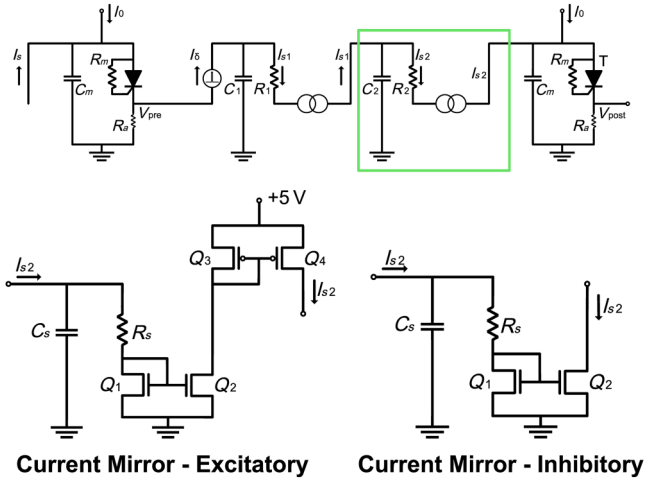

FIG. 20. The last synaptic current circuit block can be inhibitory or excitatory. For the excitatory case, Q_1, Q_2, Q_3, and Q_4 are CMOS transistors from the ALD1105PBL chip. For the inhibitory case, Q_3 and Q_4 are not used.

TABLE III. Parameters for figures.

Figure no.	Theoretical model parameters	Hardware model counterparts	Timescales
Fig. 2	C_m	0.1 μF	$\tau_m \approx 68$ ms
	R_m	680 kΩ	
	R_a	2 kΩ	$\tau_a \approx 200$ μs
Fig. 4	C_m, R_m, R_a	same as Fig. 2	
	R_W	10 kΩ	
	C_s	22 nF	$\tau_s = 1.8$ ms
	R_s	82 kΩ	
Fig. 5	C_m, R_m, R_a	same as Fig. 2	
	R_W	10 kΩ	
	C_s for (a)	47 μF	(a) $\tau_s = 4.7$ s
	C_s for (b) and (c)	1 μF	(b,c) $\tau_s = 100$ ms
	R_s	100 kΩ	
Fig. 6	C_m, R_m, R_a	same as Fig. 2	
	R_W	5 kΩ	
	C_s	4.7 μF	$\tau_s = 470$ ms
	R_s	100 kΩ	
Fig. 9	C_m, R_m, R_a	same as Fig. 2	
	R_W, C_s, R_s	same as Fig. 8	
Fig. 10	C_m, R_m, R_a	same as Fig. 2	
	R_W, C_s, R_s	same as Fig. 8	
Fig. 11	C_m	33 nF	$\tau_m \approx 22.4$ ms
	R_m	680 kΩ	
	R_a	2 kΩ	$\tau_a \approx 66$ μs
	C_s	10 μF	$\tau_s = 1$ s
	R_s	100 kΩ	
	R_W	2.2 kΩ	
	I_0	92.8 μA	
Fig. 12	C_m, R_m, R_a	same as Fig. 11	
	C_s, R_s, R_W	same as Fig. 11	
	I_0	92.8 μA	
Fig. 13	C_m, R_m, R_a	same as Fig. 11	
	C_s, R_s, R_W	same as Fig. 11	
	I_0	53.2 μA	
Fig. 14	C_m, R_m, R_a	same as Fig. 11	
	self-synapse C_s, R_s	same as Fig. 11	$\tau_{\text{ssi}} = 1$ s
	self-synapse R_W	0.27 kΩ	
	projection C_s, R_s	10 nF, 100 kΩ	$\tau_{\text{spi}} = 1$ ms
	projection R_W	1.5 kΩ	
	R_W	4.7 Ω	
	N1 I_0	62.0 μA	
	N2 I_0	46.5 μA	
Fig. 15	C_m, R_m, R_a	same as Fig. 11	
	self-synapse C_s, R_s	4.7 μF, 100 kΩ	$\tau_{\text{ssi}} = 470$ ms
	self-synapse R_W	100 Ω	
	projection C_s, R_s	1 μF, 100 kΩ	$\tau_{\text{spi}} = 100$ ms
	projection R_W	0.4 Ω	
	N1 I_0	78.8 μA	
	N2 I_0	70.6 μA	

Continued.

TABLE III. (Continued.)

Figure no.	Theoretical model parameters	Hardware model counterparts	Timescales
Fig. 16	C_m, R_m, R_a	same as Fig. 11	
	self-synapse C_s, R_s	4.7 μF, 100 kΩ	
	self-synapse R_W	100 Ω	
	projection C_s, R_s	1 μF, 100 kΩ	
	projection R_W	0.4 Ω	
	N1 I_0	57.3 μA	
	N2 I_0	52.4 μA	

linearly with $V_C(t) \approx (I_0/C_m)t$, hence the gate current follows the simple expression $I_G(t) \approx V_C/R_m = (I_0/R_mC_m)t = I_0(t/\tau_m)$. The condition to fire a spike is that the gate current overcomes its switching threshold $I_G > I_{GT}$. Hence, $I_G \approx 2\ \mu\text{A} = I_0\text{ISI}/\tau_m$, where ISI is the interspike interval. Thus, the firing rate results in $f\ (I_0) \approx (I_0/2\ \mu\text{A})/\tau_m$. For typical values of $I_0 = 60\ \mu\text{A}$, $R_m = 1\ \text{M}\Omega$, and $C_m = 1\ \mu\text{F}$, we get $f \approx 30$ Hz, which is biocompatible.

2. Synaptic block

The detailed circuit that implements the green blocks of the schematic model of Fig. 3 is shown in Fig. 19. The components are listed in Table II. The circuit implements the leaky integration of the input with a timescale given by $\tau_s = R_sC_s$.

This circuit equation is

$$dq/dt = -q/\tau_s + i_{\text{in}}, \tag{A1}$$

hence

$$dV_C/dt = -V_C/\tau_s + i_{\text{in}}/C_s \tag{A2}$$

and

$$\tau_s\, dI_R/dt = -I_R + i_{\text{in}}, \tag{A3}$$

which is exactly the form of Eqs. (2), (3), (11), and (12) of the main text. Note that, if $i_{\text{in}}(t) = I_0\delta(t)$, then $I_R(t) \propto \exp(-t/\tau_s)$; and if $i_{\text{in}}(t) = \exp(-t/\tau_s)$, then $I_R(t) \propto \alpha(-t/\tau_s)$. This is as discussed in the main text.

The key feature that one needs to achieve with the circuit to implement the system of equations is to capture the feature of successive stage current integration. Therefore, one needs to reproduce or mirror the output current on one block as the input for the next block. As was explained in the main text, this is achieved with a standard solution, namely a current mirror. We implemented this using again the ALD1105PBL chip.

We may note that there is a price to pay for adopting this simple solution. The R_s is not connected directly to the ground, as the equations above require, but to the gate of the NMOS pair Q_1–Q_2 in Fig. 19. This introduces an approximation, since the approximated expression for the output current becomes $I_{R_s} \approx (V_C - 0.7V)/R_s$.

Nevertheless, as shown in the synaptic current traces in Fig. 3, the two stages are well approximated by the exponential and the alpha functional forms, which in practice demonstrates that the circuit generates the appropriate waveforms.

Finally, notice that the output current is positive or excitatory (i.e., outgoing), hence this block implements an excitatory synaptic current. The excitatory synaptic circuit can be easily modified to implement the inhibitory synaptic current case. It is sufficient to take out half of the current mirror, so the output becomes a "sink to ground" of a current of magnitude identical to its input. Hence, this would be a negative or inhibitory current; if connected to a neuron, it would decrease the charge of the membrane C_m. The circuit implementation is shown in Fig. 20.

With these synaptic blocks, we can realize the four model synaptic currents that we discussed in the text, as follows. For the AMPA, i.e., excitatory exponential type, adopt one block (Fig. 19). For the NMDA, i.e., excitatory alpha type, adopt two identical blocks (Fig. 19). For the GABA_a, i.e., inhibitory exponential type, adopt one block (Fig. 20). For the GABA_b, i.e., inhibitory alpha type, adopt two blocks, the first stage (Fig. 19) and the second stage (Fig. 20).

3. Model parameters

In Table III, we list all the theoretical model parameters and their counterparts in the hardware model.

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