ANALOG DIVIDER

FEATURES
- HIGH ACCURACY
  0.25% maximum error, 40:1 denominator range
- TWO-QUADRANT OPERATION
  Dedicated log-antilog technique
- EASY TO USE
  Laser-trimmed to specified accuracy - no external resistors needed
- LOW COST
- DIP PACKAGE

APPLICATIONS
- DIVISION
- SQUARE ROOT
- RATIO METRIC MEASUREMENT
- PERCENTAGE COMPUTATION
- TRANSODUCER AND BRIDGE LINEARIZATION
- AUTOMATIC LEVEL AND GAIN CONTROL
- VOLTAGE CONTROLLED AMPLIFIERS
- ANALOG SIMULATION

DESCRIPTION
The DIV100 is a precision two-quadrant analog divider offering superior performance over a wide range of denominator input. Its accuracy is nearly two orders of magnitude better than multipliers used for division. It consists of four operational amplifiers and loggers transistors integrated into a single monolithic circuit and a laser-trimmed, thin-film resistor network. The electrical characteristics of these devices offer the user guaranteed accuracy without the need for external adjustment - the DIV100 is a complete, single-package analog divider.

For those applications requiring higher accuracy, the DIV100 provides the capability for optional adjustment. These adjustments allow the user to set scale factor, feedthrough, and output-referred offsets for the lowest total divider error. The DIV100 also gives the user a precision, temperature-compensated reference voltage for external use.

Designers of industrial process control systems, analytical instruments, or biomedical instrumentation will find the DIV100 easy to use and also a low cost, but highly accurate solution to their analog divider applications.
### SPECIFICATIONS

**ELECTRICAL**

Specifications at T_A = +25°C and ±VCC = ±5VDC unless otherwise noted.

<table>
<thead>
<tr>
<th>MODEL</th>
<th>CONDITION</th>
<th>DIV100UP</th>
<th>DIV100UP</th>
<th>DIV100UP</th>
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<tbody>
<tr>
<td><strong>PARAMETER</strong></td>
<td></td>
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<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td><strong>TRANSFER FUNCTION</strong></td>
<td></td>
<td>V_0 = 10V/D</td>
<td></td>
<td></td>
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<tr>
<td><strong>ACCURACY</strong></td>
<td>R_L &gt; 10kΩ</td>
<td></td>
<td></td>
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<tr>
<td>Total Error</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Initial</td>
<td>0.25V &lt; D &lt; 10V, N ≤ D</td>
<td>0.7</td>
<td>1.0</td>
<td>0.3</td>
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<tr>
<td>vs. Temperature</td>
<td>1V ≤ D &lt; 10V, N ≤ D</td>
<td>0.02</td>
<td>0.05</td>
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<td>vs. Supply</td>
<td>0.25V &lt; D &lt; 10V, N ≤ D</td>
<td>0.06</td>
<td>0.2(11)</td>
<td>0.06</td>
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<td></td>
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<td><strong>AC PERFORMANCE</strong></td>
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<tr>
<td>D = ±10V</td>
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<tr>
<td>Small-Signal Bandwidth</td>
<td>-3dB</td>
<td></td>
<td>350</td>
<td></td>
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<tr>
<td>0.5% Amplitude Error</td>
<td>Small-Signal</td>
<td>15</td>
<td></td>
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<tr>
<td>0.5% Vector Error</td>
<td>Small-Signal</td>
<td>1000</td>
<td></td>
<td></td>
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<tr>
<td>Full-Power Bandwidth</td>
<td>V_o = ±10V, I_o = ±5mA</td>
<td>30</td>
<td></td>
<td></td>
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<tr>
<td>Slew Rate</td>
<td>V_o = ±10V, I_o = ±5mA</td>
<td>15</td>
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<tr>
<td>Settling Time</td>
<td>x = 1%, 3V_o = 30V</td>
<td>4</td>
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<td>Overload Recovery</td>
<td>50% Output Overload</td>
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<td><strong>INPUT CHARACTERISTICS</strong></td>
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<td></td>
<td></td>
<td></td>
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<tr>
<td>Input Voltage Range</td>
<td>N ≤ D</td>
<td>±10</td>
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<tr>
<td>Denominator</td>
<td>D &gt; ±250mV</td>
<td>+10</td>
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<tr>
<td>Input Resistance</td>
<td>Either Input</td>
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<td></td>
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<td><strong>OUTPUT CHARACTERISTICS</strong></td>
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<tr>
<td>Full-Scale Output (FSO)</td>
<td></td>
<td>±10</td>
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<tr>
<td>Rated Output Voltage</td>
<td>I_o = ±5mA</td>
<td>±10</td>
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<tr>
<td>Current</td>
<td>V_o = ±10V</td>
<td>±5</td>
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<td>Current Limit</td>
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<tr>
<td>Positive</td>
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<td>20/2</td>
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<tr>
<td>Negative</td>
<td></td>
<td>19</td>
<td>23/2</td>
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<td><strong>OUTPUT NOISE VOLTAGE</strong></td>
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<tr>
<td>D = ±10V</td>
<td>N = ±5V</td>
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<tr>
<td>D = ±250mV</td>
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<td>370</td>
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<td><strong>REFERENCE VOLTAGE CHARACTERISTICS</strong></td>
<td>R_L &gt; 10MΩ</td>
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<tr>
<td>Output Voltage</td>
<td>Initial</td>
<td>At +25°C</td>
<td>8.3kΩ</td>
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<tr>
<td>vs. Supply</td>
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<tr>
<td>Temperature Coefficient</td>
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<tr>
<td>Output Resistance</td>
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<td>3</td>
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<td><strong>POWER SUPPLY REQUIREMENTS</strong></td>
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<tr>
<td>Rated Voltage</td>
<td>Operating Range</td>
<td>Derated Performance</td>
<td>12</td>
<td>±15</td>
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<td>Quiescent Current</td>
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<td>Positive Supply</td>
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<tr>
<td>Negative Supply</td>
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<td>100</td>
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<td><strong>AMBIENT TEMPERATURE RANGE</strong></td>
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<td>Specification</td>
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<td>Derated Performance</td>
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<td>Storage</td>
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<td>−40</td>
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*Same as DIV100UP*

**NOTES:**

1. FSO is the abbreviation for Full Scale Output.
2. This parameter is undefined and is not guaranteed. This specification is established to a 95% confidence level.
3. See General Information section for discussion.
4. For supply voltages less than ±5VDC, the absolute maximum input voltage is equal to the supply voltage.
5. Short-circuit may be to ground only. Rating applies to an ambient temperature of +38°C at rated supply voltage.

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Supply</td>
<td>±30VDC</td>
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<tr>
<td>Internal Power Dissipation</td>
<td>≤600mW</td>
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<tr>
<td>Input Voltage Range m</td>
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<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +125°C</td>
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<tr>
<td>Operating Temperature Range</td>
<td>−25°C to +85°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10 seconds)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Output Short-Circuit Duration</td>
<td>Continuous</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>+178°C</td>
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</table>
TYPICAL PERFORMANCE CURVES

PIN CONFIGURATION

1. Gain Error Adjust
2. Output
3. VCC
4. D Input Offset Adjust
5. Internally Connected to Pin 1
6. Internally Connected to Pin 14
7. Internally Connected to Pin 8
8. Reference Voltage
9. Denominator - D Input
10. Common
11. N Input Offset Adjust
12. Output Offset Adjust
13. Numerator - N Input
14. VCC

MECHANICAL

ORDER NUMBER
DIV100KP
DIV100JP
DIV100KP

CASE Epoxy
WEIGHT 2.7 Grams
CONNECTOR 014SC

NOTE
Leads in true position within 0.10 x 0.25mm R at MMC at seating plane
Denotes Pin 1

Pin numbers shown for reference only. Numbers are not marked on package

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DEFINITIONS

TRANSFER FUNCTION
The ideal transfer function for the DIV100 is:

\[ V_{out} = \frac{N}{D} \cdot V \]

where:  
- \( N \) = Numerator input voltage  
- \( D \) = Denominator input voltage  
- 10 = Internal scale factor

Figure 1 shows the operating region over the specified numerator and denominator ranges. Note that below the minimum denominator voltage (250mV) operation is undefined.

FIGURE 1. Operating Region.

ACCURACY
Accuracy is specified as a percentage of full-scale output (FSO). It is derived from the total error specification.

TOTAL ERROR
Total error is the deviation of the actual output from the ideal quotient \( 10N \). Expressed in percent of FSO(10V): e.g., for the DIV100:

\[ V_{out \, total} = V_{out \, ideal} \pm \text{total error} \]

where:  
- Total error = 0.25\%  
- FSO = 25mV.

It represents the sum of all error terms normally associated with a divider: numerator nonlinearity, denominator nonlinearity, scale-factor error, output-referred numerator and denominator offsets, and the offset due to the output amplifier. Individual errors are not specified because it is their sum that affects the user's application.

SMALL-SIGNAL BANDWIDTH
Small-signal bandwidth is the frequency the output drops to 70\% (3dB) of its DC value. The input signal must be low enough in amplitude to keep the divider's output from becoming slew-rate limited. A rule-of-thumb is to make the output voltage 100mV, p-p, when testing this parameter. Small-signal bandwidth is directly proportional to the denominator magnitude as described in the Typical Performance Curves.

0.5\% AMPLITUDE ERROR
At high frequencies, the input-to-output relationship is a complex function that produces both a magnitude and vector error. The 0.5\% amplitude error is the frequency at which the magnitude of the output drops 0.5\% from its DC value.

0.5\% VECTOR ERROR
The 0.5\% vector error is the frequency at which a phase error of 0.01 radians occurs. This is the most sensitive measure of dynamic error of a divider.

LINEARITY
Defining linearity for a nonlinear device may seem unnecessary; however, by keeping one input constant, the output becomes a linear function of the remaining input. The denominator is the input that is held fixed with a divider. Nonlinearities in a divider add harmonic distortion to the output in the amount of:

\[ \text{Percent Distortion} = \frac{\text{Percent Nonlinearity}}{\sqrt{2}} \]

FEEDTHROUGH
Feedthrough is the signal at the output for any value of denominator within its rated range, when the numerator input is zero. Ideally, the output should be zero under this condition.

GENERAL INFORMATION

WIRING PRECAUTIONS
In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a \( 10\mu F \) tantalum capacitor in parallel with a 1000\( pF \) ceramic capacitor from the \(+V_1\) and \(-V_1\) pins to the power supply common. The connection of these capacitors should be as close to the DIV100 as practical.

CAPACITIVE LOADS
Stable operation is maintained with capacitive loads of up to 1000\( pF \). Higher capacitive loads can be driven if a 220\( \Omega \) carbon resistor is connected in series with the DIV100's output.

OVERLOAD PROTECTION
The DIV100 can be protected against accidental power supply reversals by putting a diode \( D1 \) in series with each power supply line as shown in Figure 2. This precaution is necessary only in power systems that momentarily reverse polarity during turn-on or turn-off.

If this protection circuit is used, the accuracy of the DIV100 will be degraded by the power supply sensitivity specification. No other overload protection circuit is necessary. Inputs are internally protected against overvoltages and they are current-limited by at least a 10k\( \Omega \) series resistor. The output is protected against short circuits to power supply common only.
FIGURE 2. Overload Protection Circuit.

STATIC SENSITIVITY

No special handling is required. The DIV100 does not use MOS-type transistors. Furthermore, all external leads are protected by resistors against low energy electrostatic discharge (ESD).

INTERNAL POWER DISSIPATION

\[
egin{align*}
T_{J*} &= \text{Junction Temperature (output loaded)} \\
T_{J} &= \text{Junction Temperature (no load)} \\
T_{C} &= \text{Case Temperature} \\
T_{A} &= \text{Ambient Temperature} \\
\theta &= \text{Thermal Resistance}
\end{align*}
\]

This model is obviously not the simple one power source model that most linear device manufacturers give. It is, however, a more accurate model for a multidevice monolithic or hybrid integrated circuit.

The model in Figure 3 must be used in conjunction with the DIV100's absolute maximum ratings of internal power dissipation and junction temperature to determine the derated power dissipation capability of the package.

As an example of how to use this model, consider this problem:

Determine the highest ambient temperature at which the DIV100 may be operated with a continuous short circuit to ground. \( V_{CC} = \pm 15 \text{VDC} \).

\[
\begin{align*}
P_{D\text{MAX}} &= 600 \text{mW} \\
T_{J\text{MAX}} &= +175^\circ \text{C} \\
T_{A} &= T_{J\text{MAX}} - P_{D0} (\theta_{J} + \theta_{C}) \\
&= 175^\circ \text{C} - 18^\circ \text{C} - 119^\circ \text{C} = 38^\circ \text{C} \\
P_{D\text{MAX}} &= P_{D0} + P_{D\text{HEAT}} \\
&= 255 \text{mW} + 345 \text{mW} = 600 \text{mW}
\end{align*}
\]

The conclusion is that the device will withstand a short-circuit up to \( T_{A} = 38^\circ \text{C} \) without exceeding either the 175°C or 600 mW absolute maximum limits.

LIMITING OUTPUT VOLTAGE SWING

The negative output voltage swing should be limited to \( \pm 11 \text{V} \), maximum, to prevent polarity inversion and possible system instability. This should be done by limiting the input voltage range.

THEORY OF OPERATION

The DIV100 is a log-antilog divider consisting of four operational amplifiers and four logging transistors integrated into a single monolithic circuit. Its basic principle of operation can be seen by an analysis of the circuit in Figure 4.

\( V_{BE} = V_{T} \ln (I/I_{S}) \)

where:

\[
\begin{align*}
V_{T} &= kT/q \\
k &= \text{Boltzmann's constant} = 1.381 \times 10^{-23} \\
T &= \text{Absolute temperature in degrees Kelvin} \\
q &= \text{Electron charge} = 1.602 \times 10^{-19} \\
I &= \text{Collector current} \\
I_{S} &= \text{Reverse saturation current}
\end{align*}
\]

Applying equation (1) to the four logging transistors gives:

For \( Q_{1} \):

\[
V_{BE} = V_{B} - V_{S} = V_{T} \ln (V_{REF}/R_{X} - \ln I_{S})
\]

This leads to:

\[
V_{V} = -V_{T} \ln (V_{REF}/R_{X} - \ln I_{S})
\]

For \( Q_{2} \):

\[
V_{1} - V_{S} = V_{T} \ln (V_{REF}/R_{X} - \ln I_{S})
\]

For \( Q_{3} \):

\[
V_{3} = -V_{T} \ln (V_{REF}/R_{X} - \ln I_{S})
\]

We have now taken the logarithms of the input voltage \( V_{REF} \), \( V_{B} \), and \( V_{S} \). Applying equation (1) to \( Q_{1} \) gives:

\[
V_{1} - V_{S} = V_{T} \ln (V_{REF}/R_{X} - \ln I_{S})
\]

Assume \( V_{1} \) and \( I_{S} \) are the same for all four transistors (a reasonable assumption with a monolithic IC). Solving

\[
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\]

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FIGURE 5. DIV100 Two-Quadrant Log-Antilog Circuit.

This last equation in terms of the previously defined variables and taking the antilogarithm of the result yields:

\[ V_o = V_{ref} \frac{V_i R_2}{V_i R_1} \]

\[ V_D = V_{ref} \frac{R_2}{R_1} \]

In the DIV100, \( V_{ref} = 6.6V \), \( R_2 = R_s = R_{in} \), and \( R_1 \) is such that the transfer function is:

\[ V_s = 10^N D \]

where:
- \( N \) = Numerator Voltage
- \( D \) = Denominator Voltage

Figure 5 is a more detailed circuit diagram for the DIV100. In addition to the circuitry included in Figure 3, it also shows the resistors \((R_1, R_2, R_n, R_s, \text{and } R_{in})\) used for level-shifting. This converts the DIV100 to a two-quadrant divider.

The implementation of the transfer function is equation (3) is done using devices with real limitations. For example, the value of the \( D \) input must always be positive. If it isn't, \( Q_1 \) will no longer conduct, \( A_1 \) will become open loop, and its output and the DIV100 output will saturate. This limitation is further restricted in that if the \( D \) input is less than \( +250mV \) the errors will become substantial. It will still function, but its accuracy will be less.

Still another limitation is the value of the \( N \) input must always be equal to or less than the absolute value of the \( D \) input. From equation (3) it can be seen that if this limitation is not met \( V_s \) will try to be greater than the 10V output voltage limit of \( A_1 \).

A limitation that may not be obvious is the effect of source resistance. If the numerator or denominator inputs are driven from a source with more than 10Ω of output resistance, the resultant voltage divider will cause a significant output error. This voltage divider is formed by the source resistance and the DIV100 input resistance. With \( R_{source} = 10Ω \) and \( R_{source}(DIV100) = 25kΩ \) an error of 0.04% results. This means that the best performance of the DIV100 is obtained by driving its inputs from operational amplifiers.

Note that the reference voltage is brought out to pins 7 and 8. This gives the user a precision, temperature-compensated reference for external use. Its open-circuit voltage is \( \pm 6.6VDC \pm 0.075\% \), typically. Its Thévenin equivalent resistance is \( 3kΩ \). Since the output resistance is a relatively high value, an operational amplifier is necessary to buffer this source as shown in Figure 6. The external amplifier is necessary because current drawn through the \( 3kΩ \) resistor will affect the DIV100 scale factor.


OPTIONAL ADJUSTMENTS

Figure 7 shows the connections to make to adjust the DIV100 for significantly better accuracy over its 40-to-1 denominator range.

The adjustment procedure is:
1. Begin with \( R_1 \), \( R_2 \), and \( R_3 \) set to their mid-position.
2. With \( |N| = D = 10.000V \), \( \pm 1mV \), adjust \( R_1 \) for \( V_s = +10.000V \), \( \pm 1mV \). This sets the scale factor.
3. Set \( D \) to the minimum expected denominator voltage.
   With \( N = \), \( D \), adjust \( R_2 \) for \( V_s = -10.000V \). This adjusts the output referred denominator offset errors.
4. With \( D \) still at its minimum expected value, make \( N = D \). Adjust \( R_1 \) for \( V_s = 10.000V \). This adjusts the output referred offset errors.
5. Repeat steps 2-4 until the best accuracy is obtained.
TYPICAL APPLICATIONS

Figure 8 is applicable to each application discussed in this section, except the square root mode.

FIGURE 8. Connection Diagram - Divide Mode.

RATIO-METRIC MEASUREMENT

The DIV100 is useful for ratiometric measurements such as efficiency, elasticity, stress, strain, percent distortion, impedance magnitude, and fractional loss or gain. These ratios may be made for instantaneous, average, RMS, or peak values.

The advantage of using the DIV100 can be illustrated from the example shown in Figure 9.


The LVDT (Linear Variable Differential Transformer) weigh cell measures the force exerted on it by the weight of the material in the container. Its output is a voltage proportional to:

\[ V = \frac{F}{a} \]

where:
- \( W \) = Weight of material
- \( F \) = Force
- \( g \) = Acceleration due to gravity
- \( a \) = Acceleration (acting on body of weight \( W \))

In a fractional loss weighing system the initial value of the material can be determined by the volume of the container and the density of the material. If this value is then held on the D-input to the DIV100 for some time interval, the DIV100 output will be a measure of the instantaneous fractional loss:

\[ \text{Loss (L)} = \frac{W_{\text{instantaneous}}}{W_{\text{initial}}} \]

Note that by using the DIV100 in this application the common physical parameters of \( g \) and \( a \) have been eliminated from the measurement, thus eliminating the need for precise system calibration.

The output from a ratiometric measuring system may also be used as a feedback signal in an adaptive process control system. A common application in the chemical industry is the ratio control of a gas and liquid flow as illustrated in Figure 10.

FIGURE 10. Ratio Control of Water to Hydrochloric Gas.

PERCENTAGE COMPUTATION

A variation of the direct ratiometric measurements previously discussed is the need for percentage computation. In Figure 11 the DIV100 output varies as the percent deviation of the measured variable to the standard.

FIGURE 11. Percentage Computation.

TIME AVERAGING

The circuit in Figure 12 overcomes the fixed averaging interval and crude approximation of more conventional time averaging schemes.

FIGURE 12. Time Averaging Computation Circuit.

BRIDGE LINEARIZATION

The bridge circuit in Figure 13 is fundamental to pressure, force, strain and electrical measurements. It can have one or more active arms whose resistance is a function of the physical quantity, property, or condition that is being measured; e.g., force of compression. For the sake of explanation the bridge in Figure 13 has only one active arm.
FIGURE 13. Bridge Circuit.
The differential output voltage \( V_{\text{in}} \) is:
\[
V_{\text{in}} = V_B - V_A = \frac{V_{\text{EX}} \cdot R_A}{(2R_1 + 3R_3)(2 + \delta)}
\]
a nonlinear function of the resistance change in the active arm. This nonlinearity limits the useful span of the bridge to perhaps \( \pm 10\% \) variation in the measured parameter.

Bridge linearization is accomplished using the circuit in Figure 14. The instrumentation amplifier converts the differential output to a single-ended voltage needed to drive the divider. The voltage-divider string makes the numerator and denominator voltages:

\[
N = \frac{-V_A \cdot R_A}{(2R_1 + 3R_3)(2 + \delta)} \quad \text{and}
\]
\[
D = \frac{-2V_{\text{EX}} \cdot R_A}{(2R_1 + 3R_3)k_2 + \delta} \quad \text{respectively,}
\]

where: \( R_N = \text{DIV100 numerator input resistance} \)
\( R_D = \text{DIV100 denominator input resistance} \)

Applying these voltages to the DIV100 transfer function gives:
\[
V_N = \frac{10N}{D} \quad \frac{(2R_1 + 3R_3)(2 + \delta)}{(2R_1 + 3R_3)k_2 + \delta}
\]
which reduces to:
\[
V_N = 55
\]
if the divider's input resistances are equal.

The nonlinearity of the bridge has been eliminated and the circuit output is independent of variations in the excitation voltage.


AUTOMATIC GAIN CONTROL
A simple AGC circuit using the DIV100 is shown in Figure 15. The numerator voltage may vary both positive and negative. The divider's output is half-wave rectified and filtered by \( D_1 \), \( R_3 \), and \( C_1 \). It is then compared to the DC reference voltage. If a difference exists the integrator sends a control signal to the denominator input to maintain a constant output, thus compensating for input voltage changes.

FIGURE 15. Automatic Gain Control Circuit.

VOLTAGE-CONTROLLED FILTER
Figure 16 shows how to use the DIV100 in the feedback loop of an integrator to form a voltage-controlled filter. The transfer function is:
\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{K}{\tau S + 1}
\]
where:
\[
K = -\frac{R_2}{R_1}
\]
\[
\tau = \frac{10 R_2 C}{V_{\text{CONTROL}}}
\]
This circuit may be used as a single-pole low-pass active filter whose cutoff frequency is linearly proportional to the circuit's control voltage.

FIGURE 16. Voltage-Controlled Filter.

SQUARE ROOT

FIGURE 17. Connection Diagram for Square Root Mode.